











SBVS037P - AUGUST 2003 - REVISED DECEMBER 2015

**TPS732** 

# TPS732xx Capacitor-Free, NMOS, 250-mA Low-Dropout Regulator With Reverse Current **Protection**

#### **Features**

- Stable with No Output Capacitor or Any Value or Type of Capacitor
- Input Voltage Range: 1.7 V to 5.5 V
- Ultralow Dropout Voltage: 40 mV Typical at 250 mA
- Excellent Load Transient Response—With or Without Optional Output Capacitor
- NMOS Topology Provides Low Reverse Leakage
- Low Noise: 30 µV<sub>RMS</sub> Typical (10 kHz to 100 kHz)
- 0.5% Initial Accuracy
- 1% Overall Accuracy (Line, Load, and Temperature)
- Less Than 1-µA Maximum I<sub>O</sub> in Shutdown Mode
- Thermal Shutdown and Specified Min and Max **Current Limit Protection**
- Available in Multiple Output Voltage Versions
  - Fixed Outputs of 1.2 V to 5 V
  - Adjustable Outputs from 1.2 V to 5.5 V
  - **Custom Outputs Available**

# 2 Applications

- Portable and Battery-Powered Equipment
- Post-Regulation for Switching Supplies
- Noise-Sensitive Circuitry such as VCOs
- Point-of-Load Regulation for DSPs, FPGAs, ASICs, and Microprocessors

### 3 Description

The TPS732 family of low-dropout (LDO) voltage regulators uses an NMOS pass element in a voltagefollower configuration. This topology is stable using output capacitors with low equivalent series resistance (ESR), and even allows operation without a capacitor. The device also provides high reverse blockage (low reverse current) and ground pin current that is nearly constant over all values of output current.

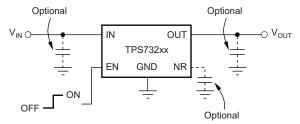
The TPS732 uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is less than 1 µA and ideal for portable applications. The extremely low output noise (30  $\mu V_{RMS}$  with 0.1- $\mu F$   $C_{NR}$ ) is ideal for powering VCOs. These devices are protected by thermal shutdown and foldback current limit.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
	SOT-23 (5)	2.90 mm × 1.60 mm
TPS732xx	SOT-223 (6)	6.50 mm × 3.50 mm
	SON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Typical Application Circuit for Fixed-Voltage Versions





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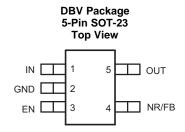
# 4 Revision History

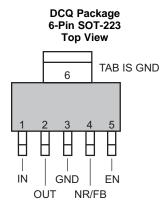
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

O.	nailiges from Revision & (August 2010) to Revision F	raye
•	Changed Features bullet about NMOS topology; deleted "new"	1
•	Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1
•	Changed first paragraph of Description section; deleted description of NMOS topology as "new"	1
•	Changed Pin Configuration and Functions section; updated table format	3
•	Changed "free-air temperature" to "junction temperature" in Absolute Maximum Ratings condition statement	4
•	Changed Thermal Information table; updated thermal resistance values for all packages	5
CI	hanges from Revision N (August, 2009) to Revision O	Page
•	Replaced the Dissipation Ratings table with the Thermal Information table	6
CI	hanges from Revision M (May, 2008) to Revision N	Page
•	Changed Figure 10	<b>7</b>
•	Added paragraph about recommended start-up sequence to Internal Current Limit section	14
•	Added paragraph about current foldback and device start-up to Enable Pin and Shutdown section	1



# 5 Pin Configuration and Functions





#### DRB Package 8-Pin SON With Exposed Thermal Pad Top View

OUT	1	¦ [8	IN
N/C	2	7	N/C
NR/FB	3	6	N/C
GND	4	5	EN

#### **Pin Functions**

	P	IN					
NAME		NO.		I/O	DESCRIPTION		
NAME	SOT-23	3 SOT-223 SON					
IN	1	1	8	I	Input supply		
GND	2	3, 6	4, Pad	_	Ground		
EN	3	5	5	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. Refer to the <i>Shutdown</i> section under <i>Feature Description</i> for more details. EN can be connected to IN if not used.		
NR	4	4	3	_	Fixed voltage versions only—connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, reducing output noise to very low levels.		
FB	4	4	3	I	Adjustable voltage version only—this pin is the input to the control loop error amplifier, and is used to set the output voltage of the device.		
OUT	5	2	1	0	Output of the regulator. There are no output capacitor requirements for stability.		

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# 6 Specifications

#### 6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
	V <sub>IN</sub>	-0.3	6	
Voltage	V <sub>EN</sub>	-0.3	6	V
vollage	V <sub>OUT</sub>	-0.3	5.5	V
	$V_{NR}, V_{FB}$	-0.3	6	
Peak output current	Гоит	Internally	y limited	
Output short-circuit duration		Indef	finite	
Continuous total power dissipation		See Power	Dissipation	
Tomporaturo	Junction range ,T <sub>J</sub>	<b>-</b> 55	150	°C
Temperature	Storage range, T <sub>stg</sub>	-65	150	C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# 6.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	
V <sub>(ESD)</sub>	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	V

#### 6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted).

		MIN	NOM MAX	UNIT
$V_{IN}$	Input supply voltage range	1.7	5.5	V
I <sub>OUT</sub>	Output current	0	250	mA
$T_J$	Operating junction temperature	-40	125	°C

JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



#### 6.4 Thermal Information

			TPS732 <sup>(3)</sup>		
	THERMAL METRIC (1)(2)	DRB [SON]	DCQ [SOT223]	DBV [SOT23]	UNIT
		8 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.3	53.1	205.9	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.8	35.2	119	
$R_{\theta JB}$	Junction-to-board thermal resistance	72.8	7.8	35.4	°C/W
ΨЈТ	Junction-to-top characterization parameter	2.7	2.9	12.7	C/VV
ΨЈВ	Junction-to-board characterization parameter	25	7.7	34.5	
R <sub>0</sub> JC(bot)	Junction-to-case (bottom) thermal resistance	5	N/A	N/A	

- (1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
- (2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
- (3) Thermal data for the DRB, DCQ, and DRV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
  - (a) i. DRB: The exposed pad is connected to the PCB ground layer through a 2 x 2 thermal via array.
    - ii. DCQ: The exposed pad is connected to the PCB ground layer through a 3 x 2 thermal via array. iii. DBV: There is no exposed pad with the DBV package.
  - (b) i. DRB: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
    - ii. DCQ: Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.
    - iii. DBV: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
  - (c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3-inch × 3-inch copper area. To understand the effects of the copper area on thermal performance, see the *Power Dissipation* section of this data sheet.

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Product Folder Links: *TPS732* 



#### 6.5 Electrical Characteristics

Over operating temperature range (T $_J$  = -40°C to 125°C),  $V_{IN}$  =  $V_{OUT(nom)}$  + 0.5  $V^{(1)}$ ,  $I_{OUT}$  = 10 mA,  $V_{EN}$  = 1.7 V, and  $C_{OUT}$  = 0.1  $\mu$ F, unless otherwise noted. Typical values are at  $T_J$  = 25°C.

PARAMETER			TE	EST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>IN</sub>	Input voltage range	(1)			1.7		5.5	V
V <sub>FB</sub>	Internal reference (	ΓPS73201)	$T_J = 25^{\circ}C$		1.198	1.2	1.21	V
	Output voltage rang	e (TPS73201) <sup>(2)</sup>			V <sub>FB</sub>	5.	5 – V <sub>DO</sub>	V
V <sub>OUT</sub>		Nominal	$T_J = 25^{\circ}C$		-0.5%		0.5%	
VO01	Accuracy <sup>(1)(3)</sup>	V <sub>IN</sub> , I <sub>OUT</sub> , and T	V <sub>OUT</sub> + 0.5 \ 10 mA ≤ I <sub>OU</sub>	/ ≤ V <sub>IN</sub> ≤ 5.5 V; <sub>T</sub> ≤ 250 mA	-1%	±0.5%	1%	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation <sup>(1)</sup>		V <sub>OUT(nom)</sub> +	0.5 V ≤ V <sub>IN</sub> ≤ 5.5 V		0.01		%/V
۸۱/	-		1 mA ≤ I <sub>OUT</sub>	≤ 250 mA		0.002		%/mA
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation		10 mA ≤ I <sub>OU</sub>	<sub>T</sub> ≤ 250 mA		0.0005		%/mA
V <sub>DO</sub>	Dropout voltage <sup>(4)</sup> (V <sub>IN</sub> = V <sub>OUT</sub> (nom) -	- 0.1 V)	I <sub>OUT</sub> = 250 r	nA		40	150	mV
$Z_{O(do)}$	Output impedance i	n dropout	1.7 V ≤ V <sub>IN</sub> :	≤ V <sub>OUT</sub> + V <sub>DO</sub>		0.25		Ω
I <sub>CL</sub>	Output current limit		V <sub>OUT</sub> = 0.9 x	∢ V <sub>OUT(nom)</sub>	250	425	600	mA
I <sub>SC</sub>	Short-circuit current		$V_{OUT} = 0 V$			300		mA
I <sub>REV</sub>	Reverse leakage cu	rrent <sup>(5)</sup> (–I <sub>IN</sub> )	V <sub>EN</sub> ≤ 0.5 V,	$0 \text{ V} \leq \text{V}_{\text{IN}} \leq \text{V}_{\text{OUT}}$		0.1	10	μA
	CND nin gurrant		I <sub>OUT</sub> = 10 m.	A (I <sub>Q</sub> )		400	550	
I <sub>GND</sub>	GND pin current		I <sub>OUT</sub> = 250 r	mA		650	950	μA
I <sub>SHDN</sub>	Shutdown current (I	GND)	V <sub>EN</sub> ≤ 0.5 V, -40°C ≤ T <sub>J</sub> ≤	V <sub>OUT</sub> ≤ V <sub>IN</sub> ≤ 5.5, ≤ 100°C		0.02	1	μΑ
I <sub>FB</sub>	FB pin current (TPS	73201)				0.1	0.3	μA
PSRR	Power-supply reject	ion ratio	f = 100 Hz,	I <sub>OUT</sub> = 250 mA		58		dB
PSKK	(ripple rejection)		f = 10 kHz, I	<sub>OUT</sub> = 250 mA		37		uБ
V	Output noise voltage	е	C <sub>OUT</sub> = 10 μ	F, No C <sub>NR</sub>	2	27 × V <sub>OUT</sub>		\/
$V_n$	BW = 10Hz - 100kH	łz	C <sub>OUT</sub> = 10 μ	F, $C_{NR} = 0.01  \mu F$	8	.5 × V <sub>OUT</sub>		$\mu V_{RMS}$
V <sub>EN(high)</sub>	EN pin high (enable	d)			1.7		$V_{IN}$	V
$V_{EN(low)}$	EN pin low (shutdov	vn)			0		0.5	V
I <sub>EN(high)</sub>	EN pin current (ena	bled)	V <sub>EN</sub> = 5.5 V			0.02	0.1	μΑ
т	Thormal shutdown t	comporatura	Shutdown	Temp increasing		160		°C
$T_{SD}$	Thermal shutdown t	emperature	Reset	Temp decreasing		140		-0
TJ	Operating junction t	emperature			-40		125	°C

# 6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>STR</sub>	Start-up time	$V_{OUT} = 3 \text{ V}, R_L = 30 \Omega$ $C_{OUT} = 1 \mu\text{F}, C_{NR} = 0.01 \mu\text{F}$		600		μs

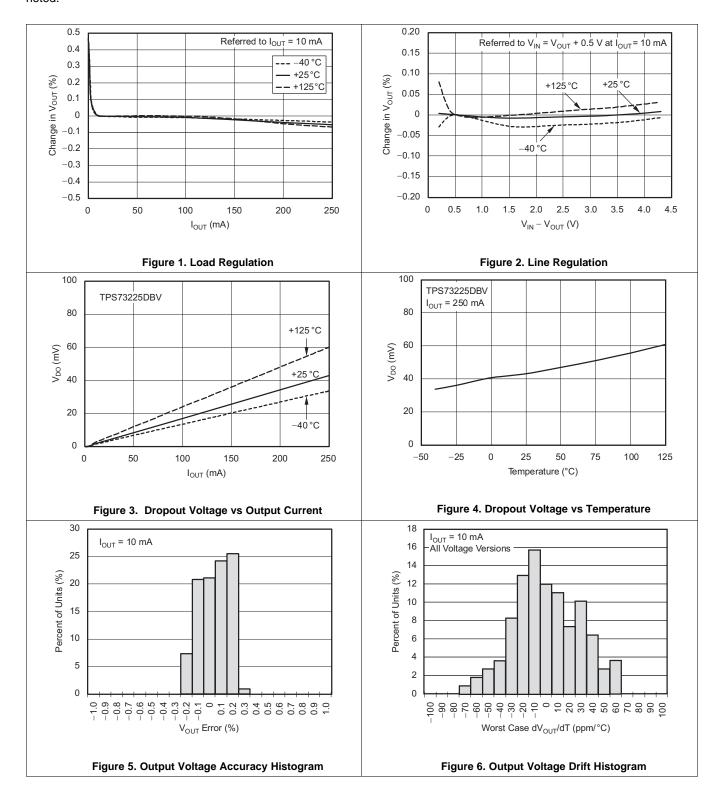
Minimum  $V_{IN} = V_{OUT} + V_{DO}$  or 1.7 V, whichever is greater. TPS73201 is tested at  $V_{OUT} = 2.5$  V. Tolerance of external resistors not included in this specification.

 $V_{DO}$  is not measured for fixed output versions with  $V_{OUT(nom)}$  < 1.8 V because minimum  $V_{IN}$  = 1.7 V. Fixed-voltage versions only; refer to *Application Information* section for more information.



#### 6.7 Typical Characteristics

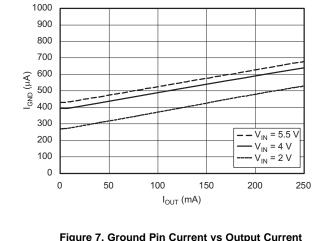
For all voltage versions at  $T_J$  = 25°C,  $V_{IN}$  =  $V_{OUT(nom)}$  + 0.5 V,  $I_{OUT}$  = 10 mA,  $V_{EN}$  = 1.7 V, and  $C_{OUT}$  = 0.1  $\mu$ F, unless otherwise noted.



# **STRUMENTS**

### **Typical Characteristics (continued)**

For all voltage versions at  $T_J = 25$ °C,  $V_{IN} = V_{OUT(nom)} + 0.5$  V,  $I_{OUT} = 10$  mA,  $V_{EN} = 1.7$  V, and  $C_{OUT} = 0.1$   $\mu$ F, unless otherwise noted.



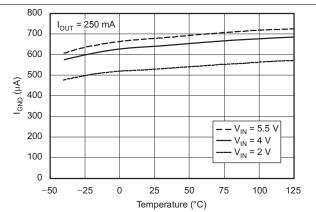
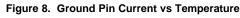
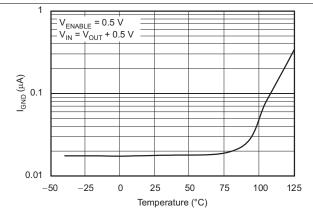


Figure 7. Ground Pin Current vs Output Current





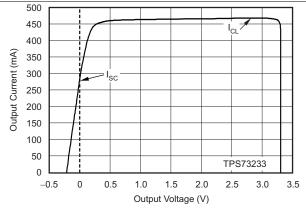


Figure 9. Ground Pin Current in Shutdown vs Temperature

Figure 10. Current Limit vs V<sub>OUT</sub> (Foldback)

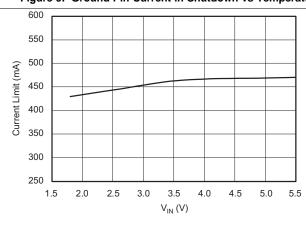


Figure 11. Current Limit vs VIN

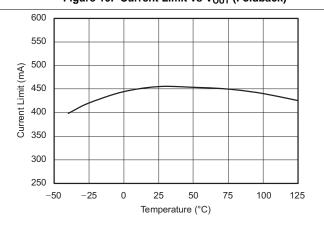
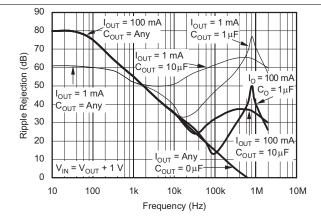


Figure 12. Current Limit vs Temperature



### **Typical Characteristics (continued)**

For all voltage versions at  $T_J = 25$ °C,  $V_{IN} = V_{OUT(nom)} + 0.5$  V,  $I_{OUT} = 10$  mA,  $V_{EN} = 1.7$  V, and  $C_{OUT} = 0.1$   $\mu F$ , unless otherwise noted.



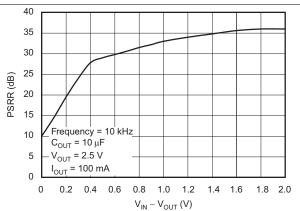
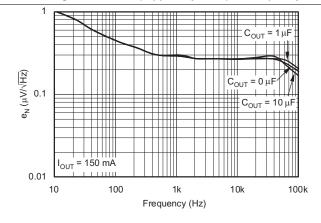


Figure 13. PSRR (Ripple Rejection) vs Frequency





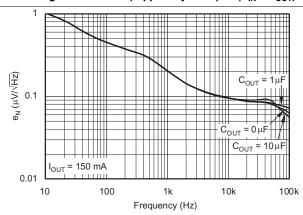
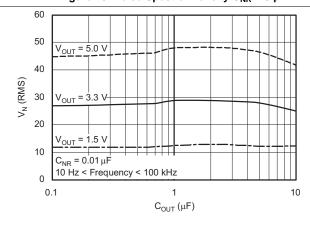


Figure 15. Noise Spectral Density  $C_{NR} = 0 \mu F$ 

Figure 16. Noise Spectral Density  $C_{NR} = 0.01 \mu F$ 



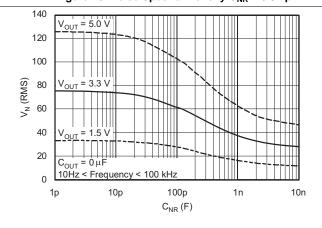


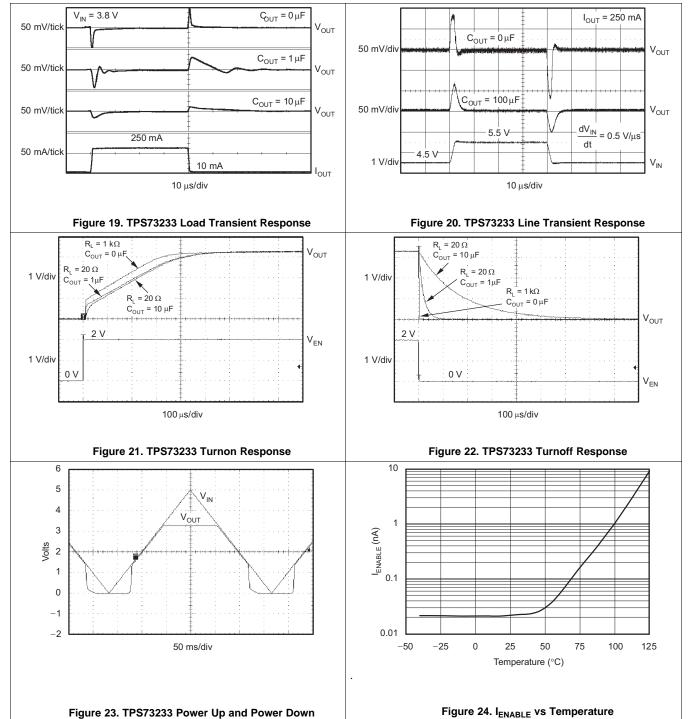
Figure 17. RMS Noise Voltage vs Cout

Figure 18. RMS Noise Voltage vs  $C_{NR}$ 



# **Typical Characteristics (continued)**

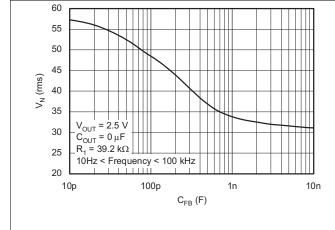
For all voltage versions at  $T_J$  = 25°C,  $V_{IN}$  =  $V_{OUT(nom)}$  + 0.5 V,  $I_{OUT}$  = 10 mA,  $V_{EN}$  = 1.7 V, and  $C_{OUT}$  = 0.1  $\mu F$ , unless otherwise noted.





# **Typical Characteristics (continued)**

For all voltage versions at  $T_J$  = 25°C,  $V_{IN}$  =  $V_{OUT(nom)}$  + 0.5 V,  $I_{OUT}$  = 10 mA,  $V_{EN}$  = 1.7 V, and  $C_{OUT}$  = 0.1  $\mu F$ , unless otherwise noted.



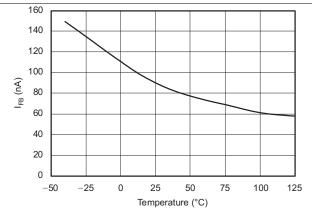
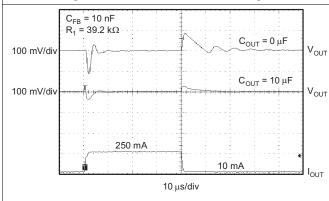


Figure 25. TPS73201 RMS Noise Voltage vs CFB





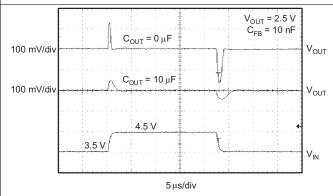


Figure 27. TPS73201 Load Transient, Adjustable Version

Figure 28. TPS73201 Line Transient, Adjustable Version



#### 7 Detailed Description

#### 7.1 Overview

The TPS732 family of low-dropout linear regulators operates down to an input voltage of 1.7 V and supports output voltages down to 1.2 V while sourcing up to 500 mA of load current. This linear regulator uses an NMOS pass element with an integrated 4-MHz charge pump to provide a dropout voltage of less than 250 mV at full load current. This unique architecture also permits stable regulation over a wide range of output capacitors. In fact, the TPS732 family of devices does not require any output capacitor for stability. The increased insensitivity to the output capacitor value and type makes this family of linear regulators an ideal choice when powering a load where the effective capacitance is unknown.

The TPS732 family of devices also features a noise reduction (NR) pin that allows for additional reduction of the output noise. With a noise reduction capacitor of 0.01  $\mu$ F connected from the NR pin to GND, the TPS73215 output noise can be as low as 12.75  $\mu$ V<sub>RMS</sub>. The low noise output featured by the TPS732 family makes the device well-suited for powering VCOs or any other noise-sensitive load.

# 7.2 Functional Block Diagrams

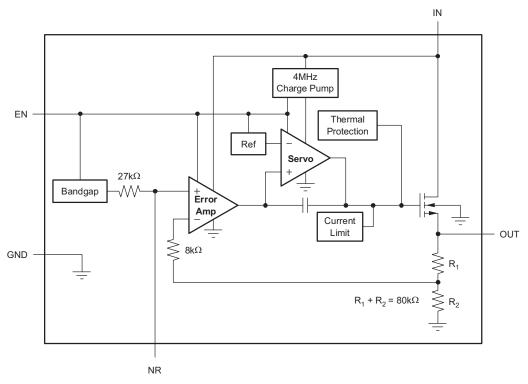


Figure 29. Fixed-Voltage Version



#### **Functional Block Diagrams (continued)**

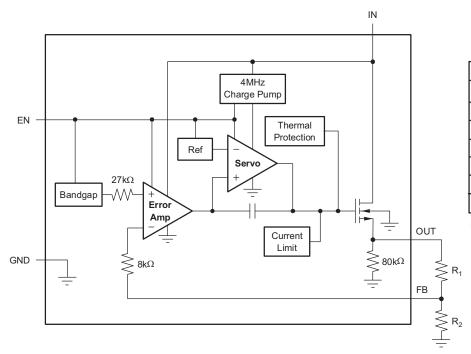


Table 1. Standard 1% Resistor Values for Common Output Voltages

Vo	R <sub>1</sub>	R <sub>2</sub>
1.2V	Short	Open
1.5V	23.2kΩ	95.3kΩ
1.8V	28.0kΩ	56.2kΩ
2.5V	39.2kΩ	36.5kΩ
2.8V	44.2kΩ	33.2kΩ
3.0V	46.4kΩ	30.9kΩ
3.3V	52.3kΩ	30.1kΩ

NOTE:  $V_{OUT}$  =  $(R_1 + R_2)/R_2 \times 1.204$ ;  $R_1 || R_2 \cong 19 \text{k}\Omega$  for best accuracy.

Figure 30. Adjustable-Voltage Version

#### 7.3 Feature Description

#### 7.3.1 Output Noise

A precision band-gap reference is used to generate the internal reference voltage,  $V_{REF}$ . This reference is the dominant noise source within the TPS732 and it generates approximately 32  $\mu V_{RMS}$  (10 Hz to 100 kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_{N} = 32\mu V_{RMS} \times \left(\frac{R_{1} + R2}{R_{2}}\right) = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}}$$

$$\tag{1}$$

Because the value of  $V_{\text{REF}}$  is 1.2 V, this relationship reduces to:

$$V_{N}(\mu V_{RMS}) = 27 \left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V)$$
(2)

An internal 27-k $\Omega$  resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor,  $C_{NR}$ , is connected from NR to ground. For  $C_{NR}$  = 10 nF, the total noise in the 10-Hz to 100-kHz bandwidth is reduced by a factor of approximately 3.2, giving the approximate relationship:

$$V_{N}(\mu V_{RMS}) = 8.5 \left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V)$$
(3)

for  $C_{NR} = 10 \text{ nF}$ .



#### **Feature Description (continued)**

This noise reduction effect is shown as RMS Noise Voltage vs  $C_{NR}$  (Figure 18) in the Typical Characteristics section.

The TPS73201 adjustable version does not have the NR pin available. However, connecting a feedback capacitor,  $C_{FB}$ , from the output to the feedback pin (FB) reduces output noise and improve load transient performance.

The TPS732 uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above  $V_{OUT}$ . The charge pump generates approximately 250  $\mu V$  of switching noise at approximately 4 MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of  $I_{OUT}$  and  $C_{OUT}$ .

#### 7.3.2 Internal Current Limit

The TPS732 internal current limit helps protect the regulator during fault conditions. Foldback current limit helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V<sub>OUT</sub> drops below 0.5 V. See Figure 10 in the *Typical Characteristics* section for a graph of I<sub>OUT</sub> vs V<sub>OUT</sub>.

Note from Figure 10 that approximately -0.2 V of  $\text{V}_{\text{OUT}}$  results in a current limit of 0 mA. Therefore, if OUT is forced below -0.2 V before EN goes high, the device may not start up. In applications that work with both a positive and negative voltage supply, the TPS732 should be enabled first.

#### 7.3.3 Enable Pin and Shutdown

The enable pin (EN) is active high and is compatible with standard TTL-CMOS levels. A  $V_{EN}$  below 0.5 V (maximum) turns the regulator off and drops the GND pin current to approximately 10 nA. When EN is used to shut down the regulator, all charge is removed from the pass transistor gate, and the output ramps back up to a regulated  $V_{OUT}$  (see Figure 21).

When shutdown capability is not required, EN can be connected to  $V_{IN}$ . However, the pass gate may not be discharged using this configuration, and the pass transistor may be left on (enhanced) for a significant time after  $V_{IN}$  has been removed. This scenario can result in reverse current flow (if the IN pin is low impedance) and faster ramp times upon power up. In addition, for  $V_{IN}$  ramp times slower than a few milliseconds, the output may overshoot upon power up.

Note that current limit foldback can prevent device start-up under some conditions. See the *Internal Current Limit* section.

#### 7.3.4 Dropout Voltage

The TPS732 uses an NMOS pass transistor to achieve extremely low dropout. When  $(V_{IN} - V_{OUT})$  is less than the dropout voltage  $(V_{DO})$ , the NMOS pass device is in its linear region of operation and the input-to-output resistance is the  $R_{DS(on)}$  of the NMOS pass element.

For large step changes in load current, the TPS732 requires a larger voltage drop from  $V_{IN}$  to  $V_{OUT}$  to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the DC dropout. Values of  $(V_{IN} - V_{OUT})$  above this line ensure normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom ( $V_{IN}$  to  $V_{OUT}$  voltage drop). Under worst-case conditions [full-scale instantaneous load change with ( $V_{IN} - V_{OUT}$ ) close to DC dropout levels], the TPS732 can take a couple of hundred microseconds to return to the specified regulation accuracy.



#### **Feature Description (continued)**

#### 7.3.5 Reverse Current

The NMOS pass element of the TPS732 provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the EN pin must be driven low before the input voltage is removed. If this is not done, the pass element may be left on due to stored charge on the gate.

After the EN pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Reverse current is specified as the current flowing out of the IN pin due to voltage applied on the OUT pin. Additional current will flow into the OUT pin due to the  $80-k\Omega$  internal resistor divider to ground (see Figure 29 and Figure 30).

For the TPS73201, reverse current may flow when  $V_{FB}$  is more than 1 V above  $V_{IN}$ .

#### 7.4 Device Functional Modes

#### 7.4.1 Normal Operation With 1.7 V $\leq$ V<sub>IN</sub> $\leq$ 5.5 V and V<sub>EN</sub> $\geq$ 1.7 V

The TPS732 family requires an input voltage of at least 1.7 V to function properly and attempt to maintain regulation.

When operating the device near 5.5 V, take care to suppress any transient spikes that may exceed the 6-V absolute maximum voltage rating. The device should never operate at a DC voltage greater than 5.5 V.

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#### 8 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

#### 8.1 Application Information

The TPS732 device belongs to a family of LDO regulators that use an NMOS pass transistor to achieve ultralow-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS732 ideal for portable applications. This regulator family offers a wide selection of fixed-output voltage versions and an adjustable-output version. All versions have thermal and overcurrent protection, including foldback current limit.

#### 8.2 Typical Applications

Figure 31 shows the basic circuit connections for the fixed-voltage models. Figure 32 gives the connections for the adjustable-voltage version (TPS73201).

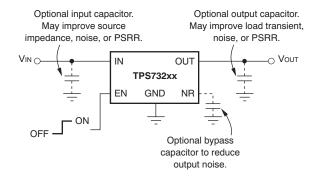


Figure 31. Typical Application Circuit for Fixed-Voltage Versions

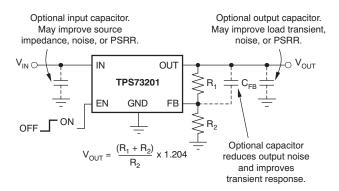


Figure 32. Typical Application Circuit for Adjustable-Voltage Version

Product Folder Links: TPS732



#### Typical Applications (continued)

#### 8.2.1 Design Requirements

For best accuracy, make the parallel combination of  $R_1$  and  $R_2$  approximately equal to 19 k $\Omega$ . This 19 k $\Omega$ , in addition to the internal 8-k $\Omega$  resistor, presents the same impedance to the error amp as the 27-k $\Omega$  bandgap reference output. This impedance helps compensate for leakages into the error amp terminals.

#### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1-µF, low ESR capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS732 does not require an output capacitor for stability and has maximum phase margin with no capacitor. It is designed to be stable for all available types and values of capacitors. In applications where multiple low ESR capacitors are in parallel, ringing may occur when the product of  $C_{OUT}$  and total ESR drops below 50 n $\Omega$ F. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance meets this requirement.

#### 8.2.2.2 Transient Response

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value 1  $\mu$ F) from the OUT pin to ground reduces undershoot magnitude but increases its duration. In the adjustable version, the addition of a capacitor,  $C_{FB}$ , from the OUT pin to the FB pin also improves the transient response.

The TPS732 does not have active pulldown when the output is overvoltage. This feature allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This feature also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor  $C_{\text{OUT}}$  and the internal/external load resistance. The rate of decay is given by:

(Fixed voltage versions)

$$dV / dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel R_{LOAD}}$$
(4)

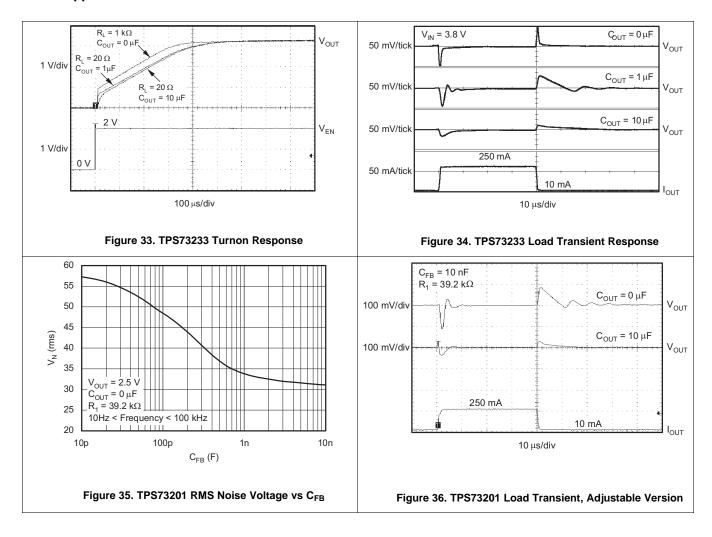
(Adjustable voltage version)

$$dV / dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel (R_1 + R_2) \parallel R_{LOAD}}$$
(5)



# **Typical Applications (continued)**

#### 8.2.3 Application Curves





#### 9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range between 1.7 V and 5.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

# 10 Layout

#### 10.1 Layout Guidelines

To improve AC performance such as PSRR, output noise, and transient response, TI recommends designing the PCB with separate ground planes for V<sub>IN</sub> and V<sub>OUT</sub>, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Solder pad footprint recommendations for the TPS732 are presented in Application Bulletin Solder Pad Recommendations for Surface-Mount Devices (SBFA015), available from the TI website at www.ti.com.

#### 10.2 Layout Examples

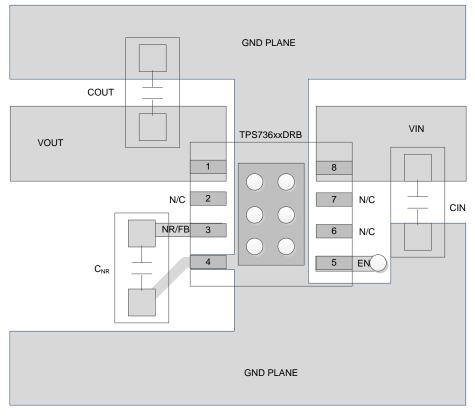


Figure 37. Fixed Output Voltage Option Layout (DRB Package)

Product Folder Links: TPS732

#### **Layout Examples (continued)**

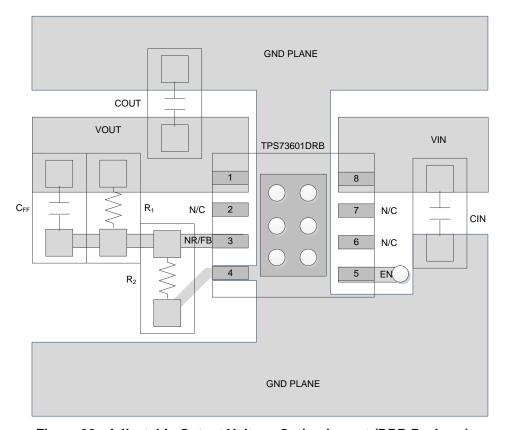


Figure 38. Adjustable Output Voltage Option Layout (DRB Package)

#### 10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS732 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS732 into thermal shutdown will degrade device reliability.



#### Thermal Considerations (continued)

#### 10.3.1 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are shown in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heat-sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation ( $P_D$ ) is equal to the product of the output current times the voltage drop across the output pass element ( $V_{IN}$  to  $V_{OUT}$ ):

$$P_{D} = (V_{IN} - V_{OUT}) \times I_{OUT}$$
(6)

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

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#### 11 Device and Documentation Support

#### 11.1 Device Support

#### 11.1.1 Development Support

#### 11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS732. The TPS73201DRBEVM-518 evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

#### 11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS732 is available through the product folders under Simulation Models.

#### 11.1.2 Device Nomenclature

Table 1. Device Nomenclature (1)

PRODUCT	V <sub>OUT</sub>
TPS732 <b>xx <i>yyy z</i></b>	XX is the nominal output voltage (for example, 25 = 2.5 V; 01 = Adjustable). YYY is the package designator. Z is the tape and reel quantity (R = 3000, T = 250).

<sup>(1)</sup> For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

# 11.2 Documentation Support

#### 11.2.1 Related Documentation

- Regulating V<sub>OUT</sub> Below 1.2 V Using an External Reference, SLVA216
- Solder Pad Recommendations for Surface-Mount Devices, SBFA019
- TPS73x01DRBEVM-518 User's Guide, SBVU014

#### 11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links** 

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS73201	Click here	Click here	Click here	Click here	Click here
TPS73213	Click here	Click here	Click here	Click here	Click here
TPS73215	Click here	Click here	Click here	Click here	Click here
TPS73216	Click here	Click here	Click here	Click here	Click here
TPS73218	Click here	Click here	Click here	Click here	Click here
TPS73219	Click here	Click here	Click here	Click here	Click here
TPS73225	Click here	Click here	Click here	Click here	Click here
TPS73230	Click here	Click here	Click here	Click here	Click here
TPS73233	Click here	Click here	Click here	Click here	Click here
TPS73250	Click here	Click here	Click here	Click here	Click here

Product Folder Links: TPS732



#### 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

#### 11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### 11.7 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

#### 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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13-Aug-2021

# **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73201DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ	Samples
TPS73201DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ	Samples
TPS73201DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ	Samples
TPS73201DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ	Samples
TPS73201DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73201	Samples
TPS73201DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	PS73201	Samples
TPS73201DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PJEQ	Samples
TPS73201DRBRG4	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PJEQ	Samples
TPS73201DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PJEQ	Samples
TPS73201DRBTG4	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PJEQ	Samples
TPS73213DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BWD	Samples
TPS73213DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BWD	Samples
TPS73215DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T38	Samples
TPS73215DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T38	Samples
TPS73215DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73215	Samples
TPS73215DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73215	Samples
TPS73216DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T50	Samples
TPS73216DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T50	Samples
TPS73218DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T37	Samples
TPS73218DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T37	Samples





13-Aug-2021 www.ti.com

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73218DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T37	Samples
TPS73218DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73218	Samples
TPS73218DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	PS73218	Samples
TPS73219DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CGE	Samples
TPS73219DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CGE	Samples
TPS73225DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T36	Samples
TPS73225DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T36	Samples
TPS73225DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T36	Samples
TPS73225DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73225	Samples
TPS73225DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73225	Samples
TPS73230DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T39	Samples
TPS73230DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T39	Samples
TPS73230DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73230	Samples
TPS73233DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T40	Samples
TPS73233DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T40	Samples
TPS73233DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73233	Samples
TPS73233DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	PS73233	Samples
TPS73250DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T41	Samples
TPS73250DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T41	Samples
TPS73250DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73250	Samples
TPS73250DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73250	Samples

# PACKAGE OPTION ADDENDUM

www.ti.com 13-Aug-2021

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF TPS732:

Automotive : TPS732-Q1

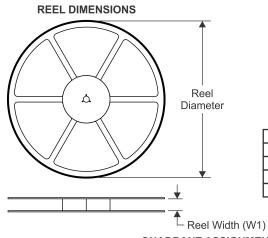
NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



www.ti.com 5-Jan-2022

#### TAPE AND REEL INFORMATION



# TAPE DIMENSIONS KO P1 BO W Cavity AO

	Α0	Dimension designed to accommodate the component width
	B0	Dimension designed to accommodate the component length
	K0	Dimension designed to accommodate the component thickness
	W	Overall width of the carrier tape
г	D1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



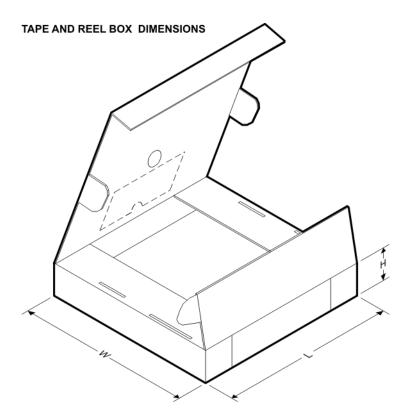
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73201DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS73201DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73201DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73201DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73201DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73201DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73201DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS73201DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS73201DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73213DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73213DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73215DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73215DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73215DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73216DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73218DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73218DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73218DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3



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Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73219DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73219DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73225DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73225DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73225DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73230DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73230DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73230DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73233DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73233DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73233DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73250DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73250DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73250DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73201DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73201DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS73201DBVT	SOT-23	DBV	5	250	200.0	183.0	25.0



# **PACKAGE MATERIALS INFORMATION**

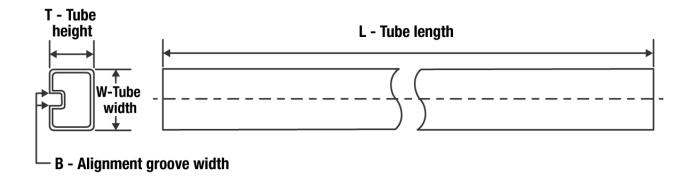
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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73201DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73201DCQR	SOT-223	DCQ	6	2500	853.0	449.0	35.0
TPS73201DRBR	SON	DRB	8	3000	853.0	449.0	35.0
TPS73201DRBR	SON	DRB	8	3000	367.0	367.0	38.0
TPS73201DRBT	SON	DRB	8	250	213.0	191.0	35.0
TPS73201DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS73213DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73213DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73215DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73215DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73215DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TPS73216DBVT	SOT-23	DBV	5	250	213.0	191.0	35.0
TPS73218DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73218DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73218DCQR	SOT-223	DCQ	6	2500	853.0	449.0	35.0
TPS73219DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73219DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73225DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73225DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73225DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TPS73230DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73230DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73230DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TPS73233DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73233DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73233DCQR	SOT-223	DCQ	6	2500	853.0	449.0	35.0
TPS73250DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73250DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73250DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0

# PACKAGE MATERIALS INFORMATION

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#### **TUBE**

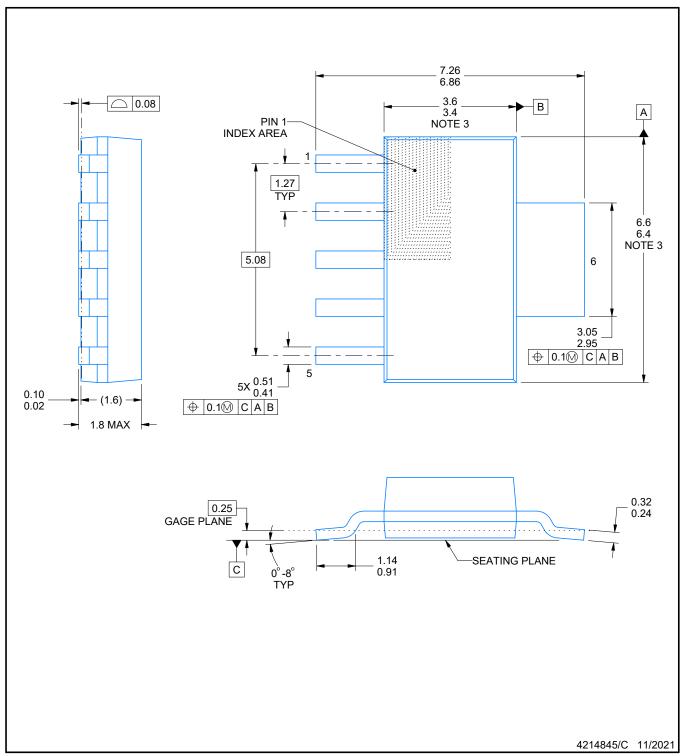


#### \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS73201DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS73215DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS73218DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS73225DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS73233DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS73250DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68



PLASTIC SMALL OUTLINE



#### NOTES:

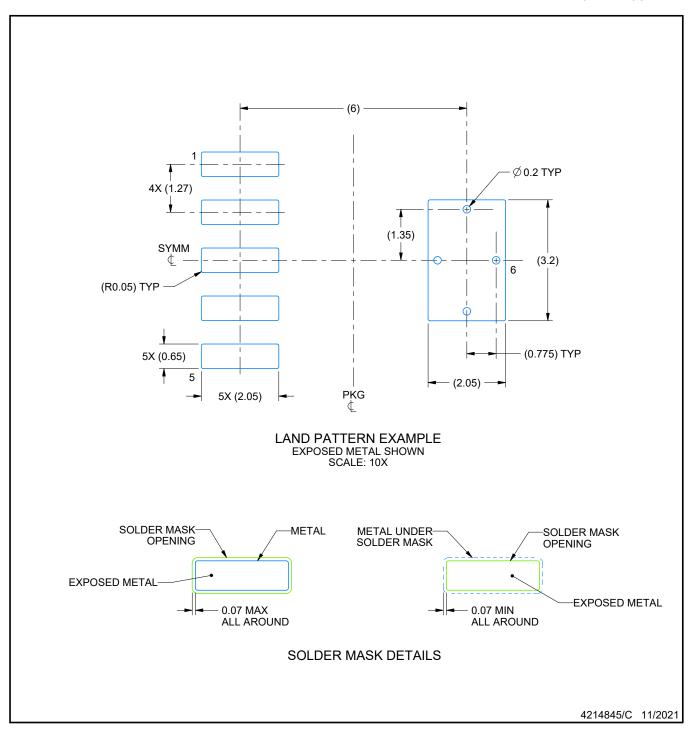
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.



PLASTIC SMALL OUTLINE

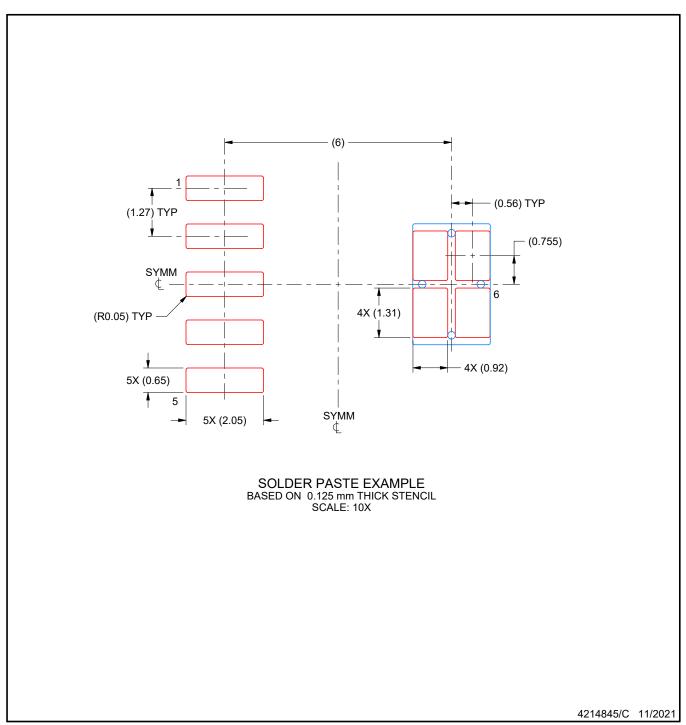


NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE TRANSISTOR



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)



<sup>7.</sup> Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

<sup>8.</sup> Board assembly site may have different recommendations for stencil design.



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4203482/L





PLASTIC SMALL OUTLINE - NO LEAD



#### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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