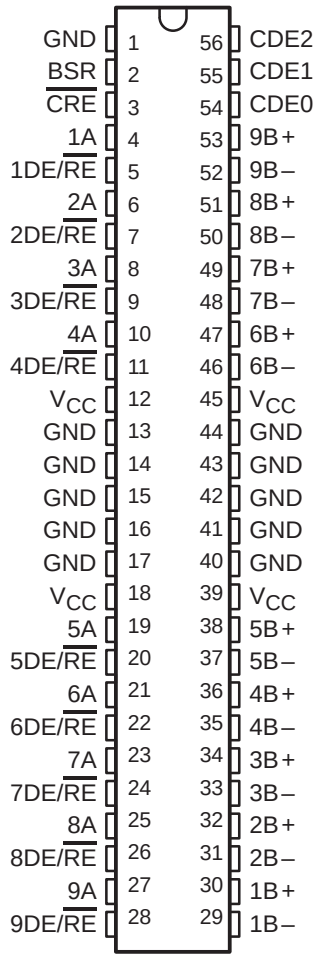
- **Nine Differential Channels for the Data and Control Paths of the Differential Small Computer Systems Interface (SCSI) and Intelligent Peripheral Interface (IPI-2)**
- **Meets or Exceeds the Requirements of ANSI Standard RS-485 and ISO 8482:1987(E)**
- **Packaged in Shrink Small-Outline Package With 25-mil Terminal Pitch**
- **Designed to Operate at 10 Million Transfers Per Second**
- **Low Disabled Supply Current 1.4 mA Typical**
- **Thermal-Shutdown Protection**
- **Power-Up/Power-Down Glitch Protection**
- **Positive and Negative Output-Current Limiting**
- **Open-Circuit Fail-Safe Receiver Design**

**DL PACKAGE**
**(TOP VIEW)**




Pins 13 through 17 and 40 through 44 are connected together to the package lead frame and signal ground.

## description

The SN75LBC976 is a nine-channel differential transceiver based on the 75LBC176 LinASIC™ cell. Use of TI's LinBiCMOS™† process technology allows the power reduction necessary to integrate nine differential transceivers. On-chip enabling logic makes this device applicable for the data path (eight data bits plus parity) and the control path (nine bits) for both the Small Computer Systems Interface (SCSI) and the Intelligent Peripheral Interface (IPI-2) standard data interfaces.

The SN75LBC976 is packaged in a shrink small-outline package (DL) with improved thermal characteristics using heat-sink terminals. This package is ideal for low-profile, space-restricted applications such as hard disk drives.

The switching speed and testing capabilities of the SN75LBC976 are sufficient to transfer data over the data bus at 10 million transfers per second. Each of the nine channels conforms to the requirements of the ANSI RS-485 and ISO 8482:1987(E) standards referenced by ANSI X3.129-1986 (IPI), ANSI X3.131-1993 (SCSI-2), and the proposed SCSI-3 standards.

The SN75LBC976 is characterized for operation from 0°C to 70°C.

† Patent pending

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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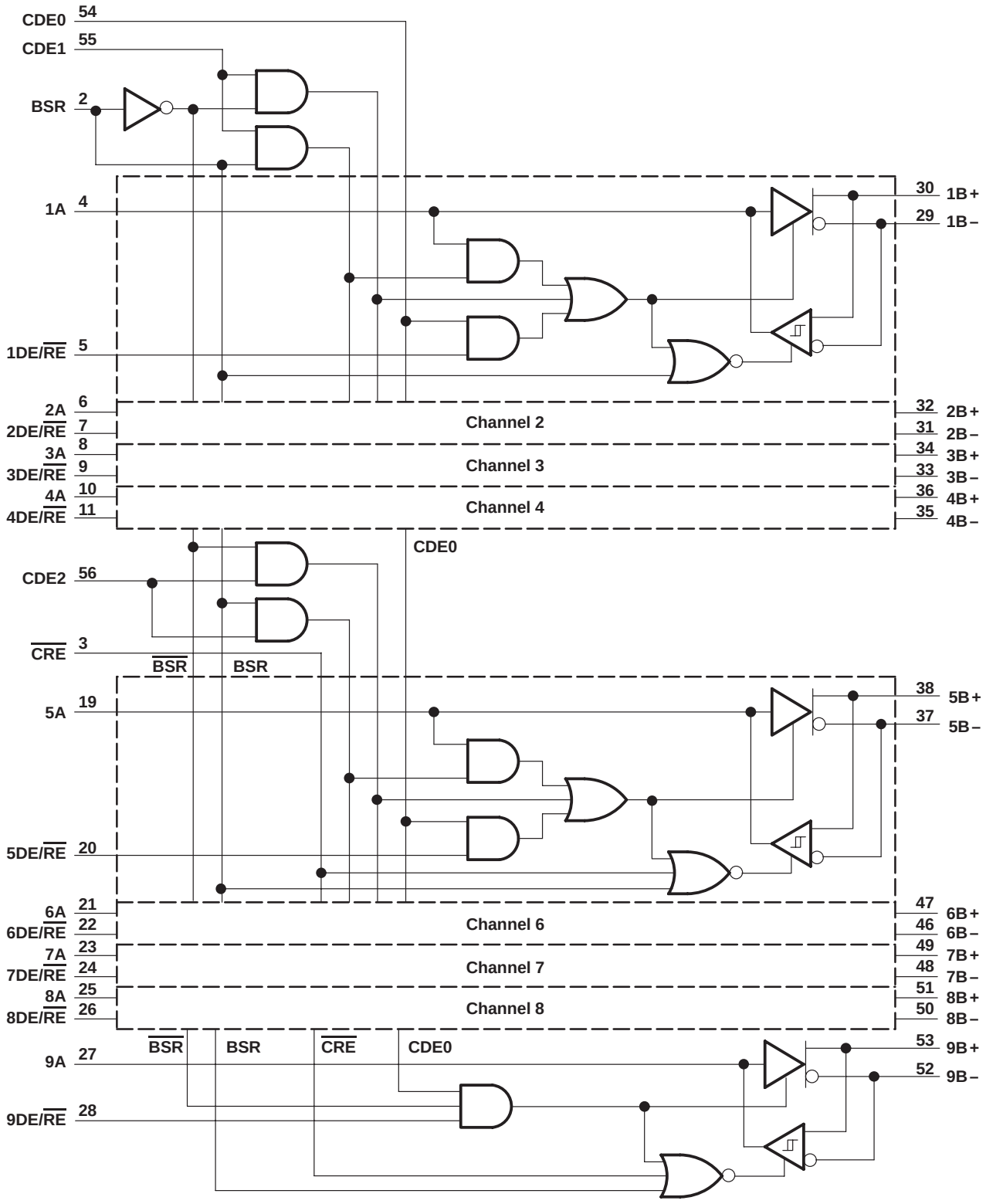
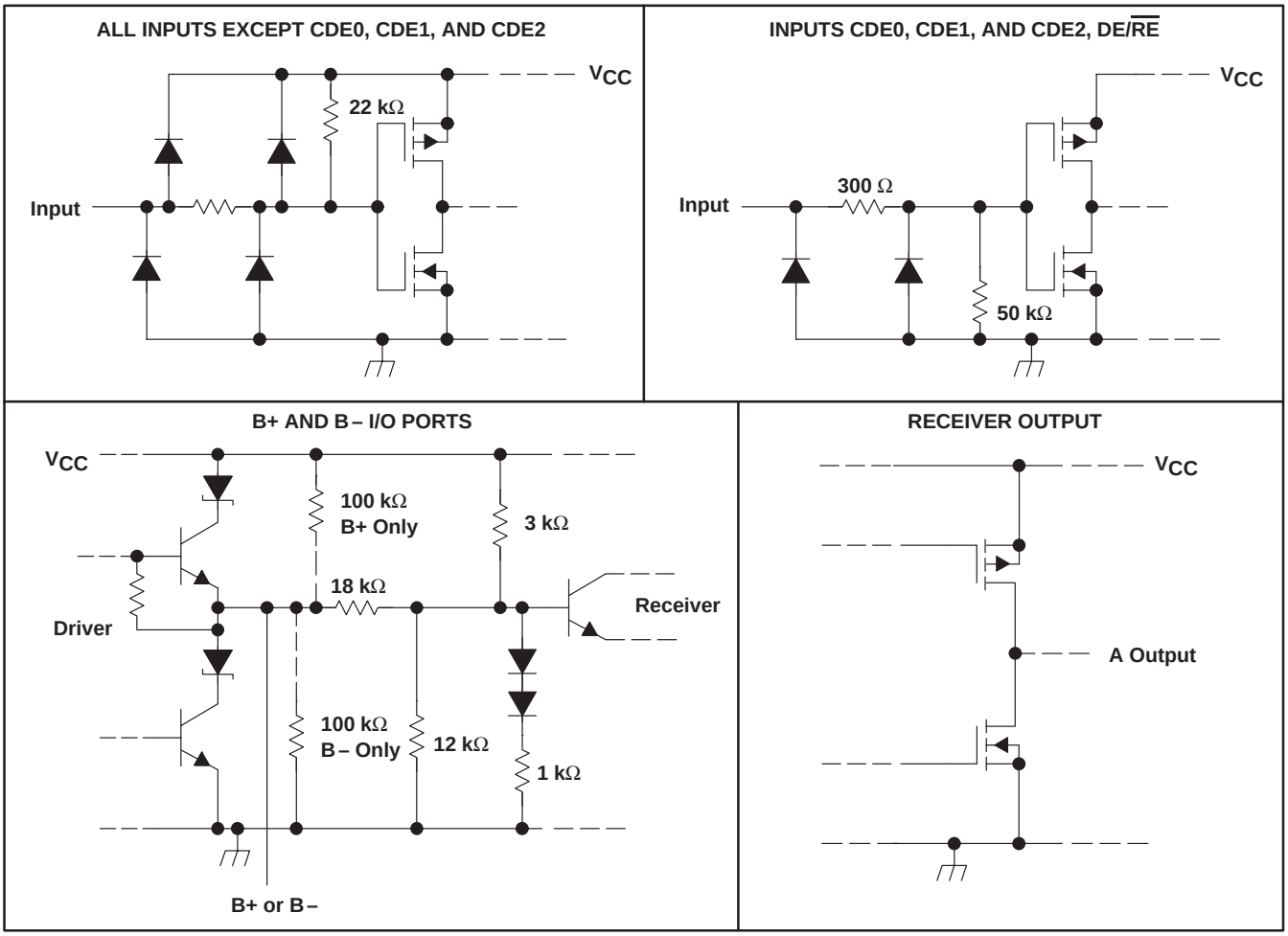
## logic diagram (positive logic)†




† For additional logic diagrams, see Application Information, Table 1 and Figures 7 through 44.

## schematics of inputs and outputs




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ (see Note 1) | –0.3 V to 7 V |
| Bus voltage range | –10 V to 15 V |
| Data I/O and control (A-side) voltage range | –0.3 V to 7 V |
| Continuous power dissipation | internally limited |
| Operating free-air temperature range, $T_A$ | 0°C to 70°C |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | 4.75 | 5 | 5.25 | V |
| Voltage at any bus terminal (separately or common-mode), $V_O$, $V_I$, or $V_{IC}$ | B+ or B– | | | 12 | V |
| | | | | –7 | |
| High-level input voltage, $V_{IH}$ | All except B+ and B– | 2 | | | V |
| Low-level input voltage, $V_{IL}$ | All except B+ and B– | | | 0.8 | V |
| High-level output current, $I_{OH}$ | B+ or B– | | | –60 | mA |
| | A | | | –8 | mA |
| Low-level output current, $I_{OL}$ | B+ or B– | | | 60 | mA |
| | A | | | 8 | mA |
| Operating free-air temperature, $T_A$ | | 0 | | 70 | °C |

## device electrical characteristics over recommended ranges of operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{IH}$ | High-level input current | BSR, A, DE/$\overline{RE}$, and $\overline{CRE}$ | See Figure 1 | $V_{IH}$ = 2 V | | | –200 | µA |
| | | CDE0, CDE1, and CDE2 | | | | | 100 | µA |
| $I_{IL}$ | Low-level input current | BSR, A, DE/$\overline{RE}$, and $\overline{CRE}$ | | $V_{IL}$ = 0.8 V | | | –200 | µA |
| | | CDE0, CDE1, and CDE2 | | | | | 100 | µA |
| $I_{CC}$ | Supply current | All drivers and receivers disabled | BSR and CDE0 at 5 V, Other inputs at 0 V | | | 1.4 | 3 | mA |
| | | All receivers enabled | No load, $V_{ID}$ = 5 V, All other inputs at 0 V | | | 29 | 45 | mA |
| | | All drivers enabled | BSR at 0 V, No load, All other inputs at 5 V | | | 4.8 | 10 | mA |
| $C_O$ | Bus port output capacitance | | B+ or B– | | | 16 | | pF |
| $C_{pd}$ | Power dissipation capacitance‡ | | One driver | | | 460 | | pF |
| | | | One receiver | | | 50 | | pF |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ $C_{pd}$ determines the no-load dynamic current consumption; $I_S = C_{pd} \cdot V_{CC} \cdot f + I_{CC}$.

## driver electrical characteristics over recommended ranges of operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $\lvert V_{OD} \rvert$ | Differential output voltage | $V_{test}$ = –7 V to 12 V, See Figure 2 | 1 | 2 | | V |
| $I_{OS}$ | Output short-circuit current | See Figure 3 | | | ±250 | mA |
| $I_{OZ}$ | High-impedance-state output current | See receiver input current | | | | |

## receiver electrical characteristics over recommended ranges of operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | | $V_{ID}$ = 200 mV, See Figure 1 | $I_{OH}$ = –8 mA, | 2.5 | | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{ID}$ = –200 mV, See Figure 1 | $I_{OL}$ = 8 mA, | | | 0.8 | V |
| $V_{IT+}$ | Positive-going input threshold voltage | | $I_{OH}$ = –8 mA, | See Figure 1 | | | 0.2 | V |
| $V_{IT-}$ | Negative-going input threshold voltage | | $I_{OL}$ = 8 mA, | See Figure 1 | –0.2 | | | V |
| $V_{hys}$ | Receiver input hysteresis voltage ($V_{IT+} - V_{IT-}$) | | | | | 45 | | mV |
| $I_I$ | Receiver input current | B+ and B– | $V_I$ = 12 V, Other input at 0 V, | $V_{CC}$ = 5 V, See Figure 1 | | 0.7 | 1 | mA |
| | | | $V_I$ = 12 V, Other input at 0 V, | $V_{CC}$ = 0, See Figure 1 | | 0.8 | 1 | mA |
| | | | $V_I$ = –7 V, Other input at 0 V, | $V_{CC}$ = 5 V, See Figure 1 | | –0.5 | –0.8 | mA |
| | | | $V_I$ = –7 V, Other input at 0 V, | $V_{CC}$ = 0, See Figure 1 | | –0.4 | –0.8 | mA |
| $I_{OZ}$ | High-impedance-state output current | | See Figure 1 | $V_O$ = GND | | | –200 | µA |
| | | | | $V_O$ = $V_{CC}$ | | | 50 | |

## driver switching characteristics over recommended operating conditions (unless otherwise noted) (see Figure 4)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{d(OD)}$ | Differential delay time, high- to low-level output ($t_{d(ODH)}$) or low- to high-level output ($t_{d(ODL)}$) | | | 7.6 | | 19.6 | ns |
| | | $V_{CC}$ = 5 V, | $T_A$ = 25°C | 9.1 | | 17.1 | |
| | | $V_{CC}$ = 5 V, | $T_A$ = 70°C | 11.5 | | 19.5 | |
| $t_{sk(lim)}$ | Skew limit, the maximum difference in propagation delay times between any two drivers on any two devices | | | | | 12 | ns |
| | | $V_{CC}$ = 5 V, | See Note 2 | | | 8 | |
| $t_{sk(p)}$ | Pulse skew ($\lvert t_{d(ODL)} - t_{d(ODH)} \rvert$) | | | | 0 | 6 | ns |
| $t_t$ | Transition time ($t_r$ or $t_f$) | | | | 10 | | ns |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

NOTE 2: This specification applies to any 5°C band within the operating temperature range.

### receiver switching characteristics over recommended operating conditions (see Figure 5) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation delay time, high- to low-level output ($t_{PLH}$) or low- to high-level output ($t_{PHL}$) | | 21.5 | | 33 | ns |
| | | $V_{CC}$ = 5 V, $T_A$ = 25°C | 22.6 | | 31.6 | |
| | | $V_{CC}$ = 5 V, $T_A$ = 70°C | 23.4 | | 32.4 | |
| $t_{sk(lim)}$ | Skew limit, the maximum difference in propagation delay times between any two drivers on any two devices | | | | 12 | ns |
| | | $V_{CC}$ = 5 V, See Note 2 | | | 9 | |
| $t_{sk(p)}$ | Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$) | | | 2 | 6 | ns |
| $t_t$ | Transition time ($t_r$ or $t_f$) | | | 3 | | ns |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
NOTE 2: This specification applies to any 5°C band within the operating temperature range.

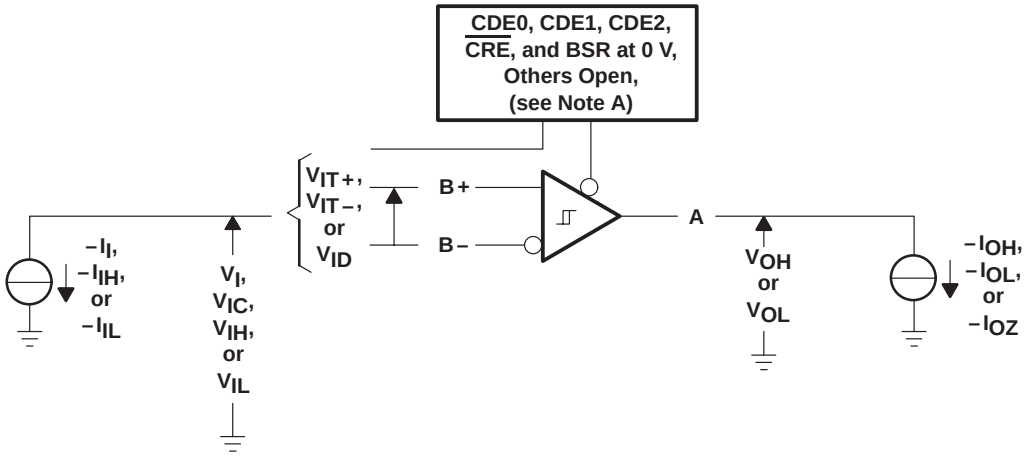
### transceiver switching characteristics over recommended operating conditions

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{en(RXL)}$ | Enable time, transmit-to-receive to low-level output | See Figure 6 | | 150 | ns |
| $t_{en(RXH)}$ | Enable time, transmit-to-receive to high-level output | | | 150 | ns |
| $t_{en(TXL)}$ | Enable time, receive-to-transmit to low-level output | | | 80 | ns |
| $t_{en(TXH)}$ | Enable time, receive-to-transmit to high-level output | | | 80 | ns |
| $t_{su}$ | Setup time, CDE0, CDE1, CDE2, BSR, or $\overline{CRE}$ to active input(s) or output(s) | | 150 | | ns |

### thermal characteristics

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-free-air thermal resistance | Board mounted, No air flow | | 50 | | °C/W |
| $R_{\theta JC}$ | Junction-to-case thermal resistance | | | 12 | | °C/W |

## PARAMETER MEASUREMENT INFORMATION




NOTE A: For the $I_{OZ}$ measurement, BSR is at 5 V and CDE0, CDE1, and CDE2 are at 0 V.

**Figure 1. Receiver Test Circuit and Input Conditions**

## PARAMETER MEASUREMENT INFORMATION

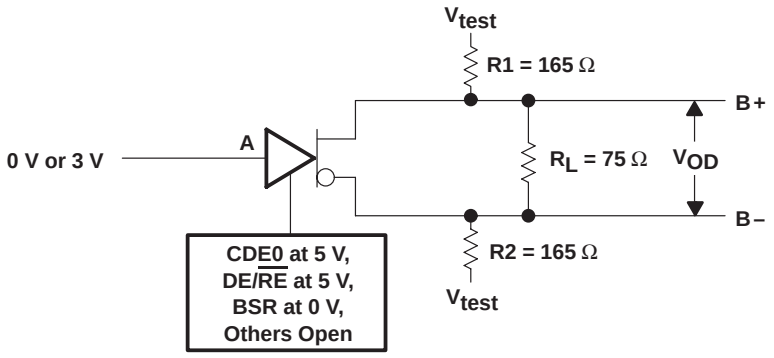
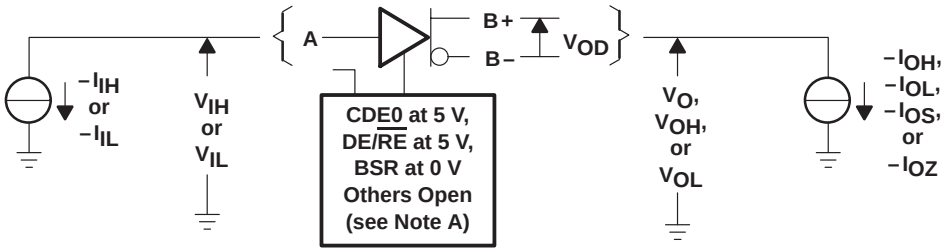


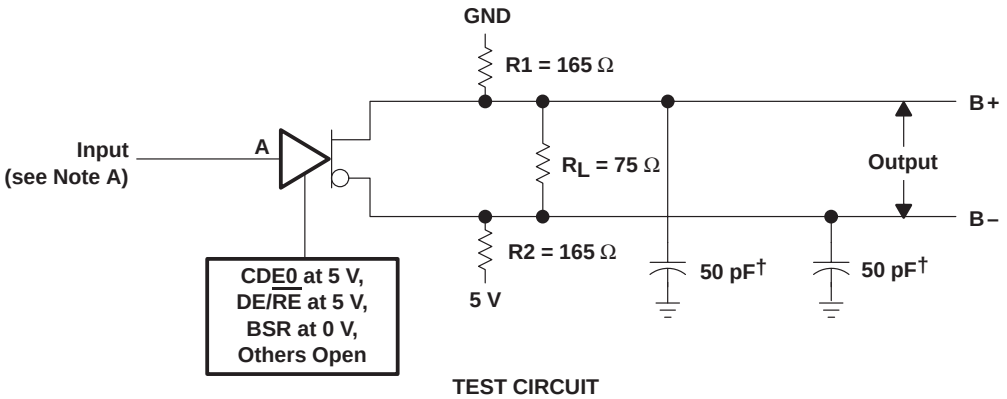

**Figure 2. Driver $V_{OD}$ Test Circuit**



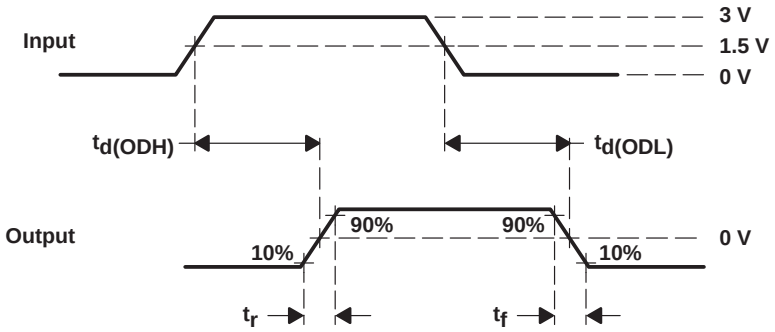

NOTE A: For the $I_{OZ}$ test, the BSR input is at 5 V and all others are at 0 V.

**Figure 3. Driver Test Circuit and Input Conditions**

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT



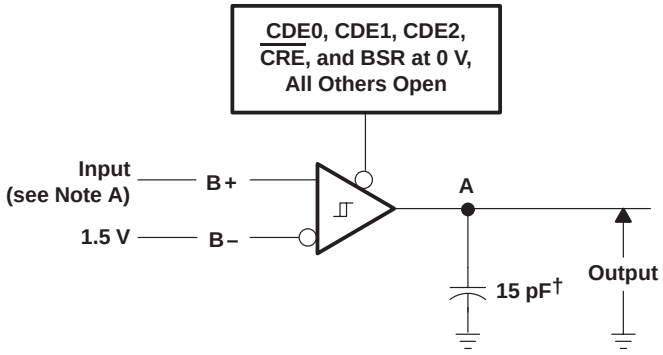

VOLTAGE WAVEFORMS

† Includes probe and jig capacitance.

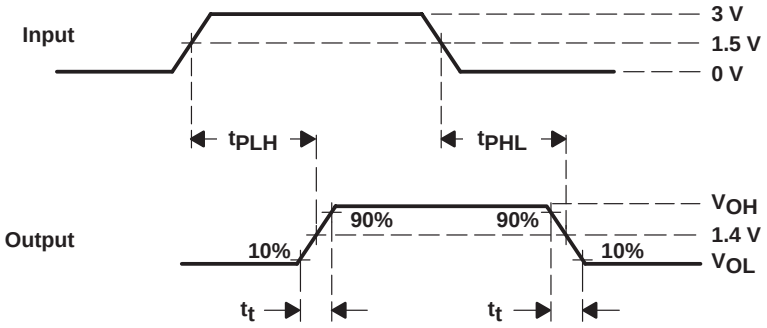
NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, $t_r$ and $t_f$ < 6 ns, and $Z_O$ = 50 Ω.

**Figure 4. Driver Test Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT



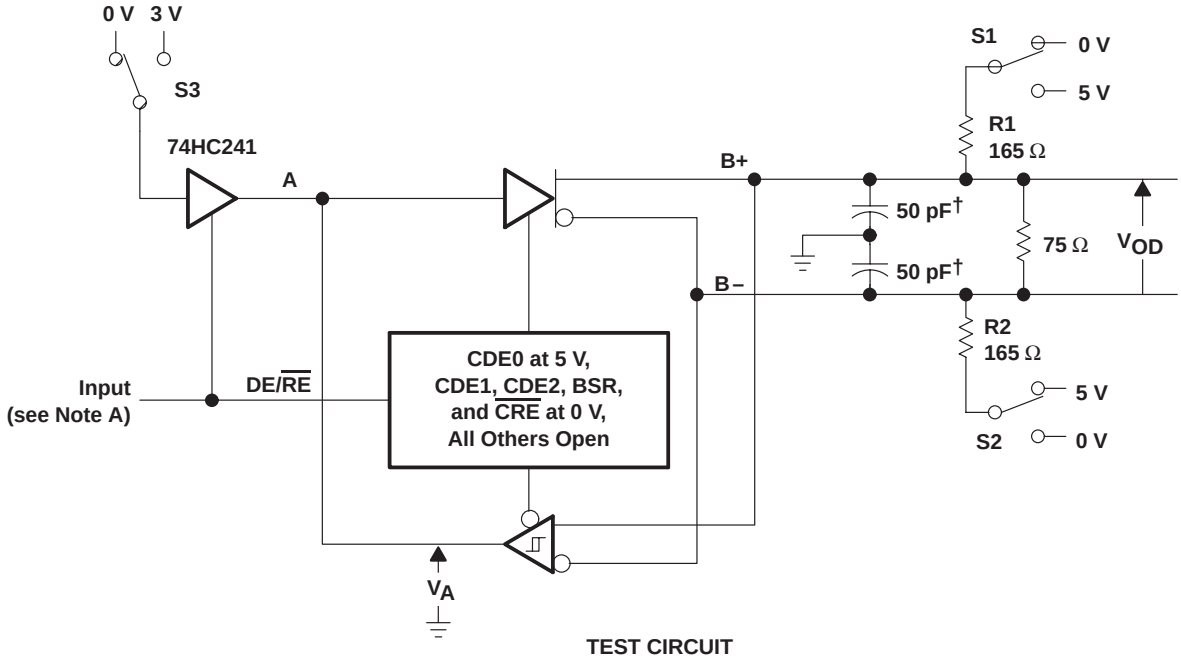

VOLTAGE WAVEFORMS

† Includes probe and jig capacitance.

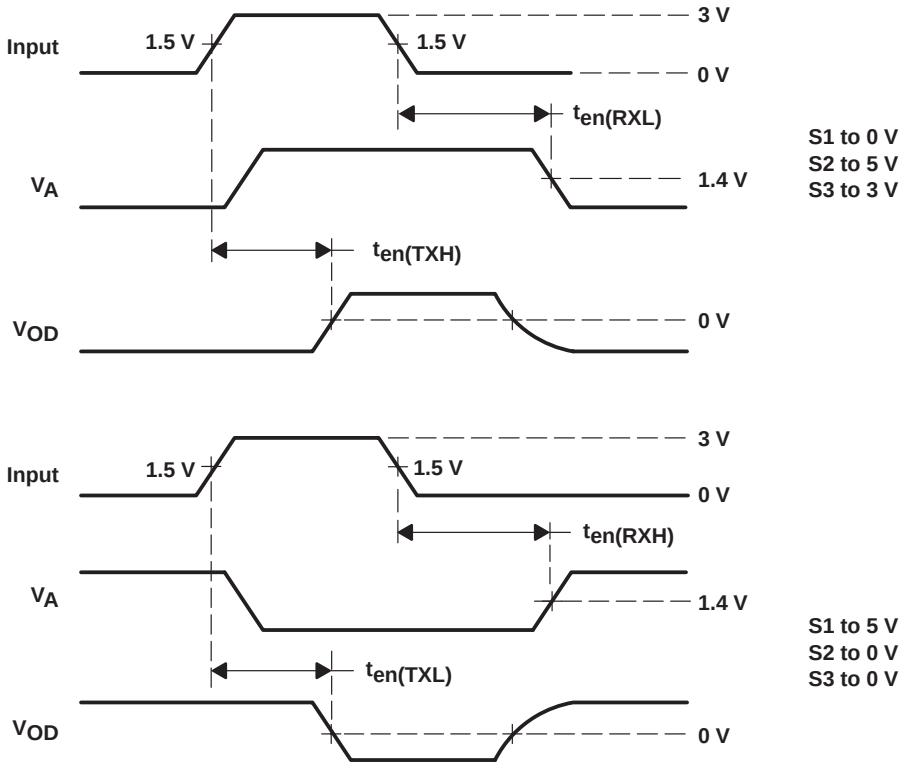
NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, $t_r$ and $t_f$ < 6 ns, and $Z_O$ = 50 Ω.

**Figure 5. Receiver Test Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT




VOLTAGE WAVEFORMS

† Includes probe and jig capacitance.

NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, $t_r$ and $t_f$ < 6 ns, and $Z_O$ = 50 Ω.

**Figure 6. Enable Time Test Circuit and Voltage Waveforms**

## TYPICAL CHARACTERISTICS

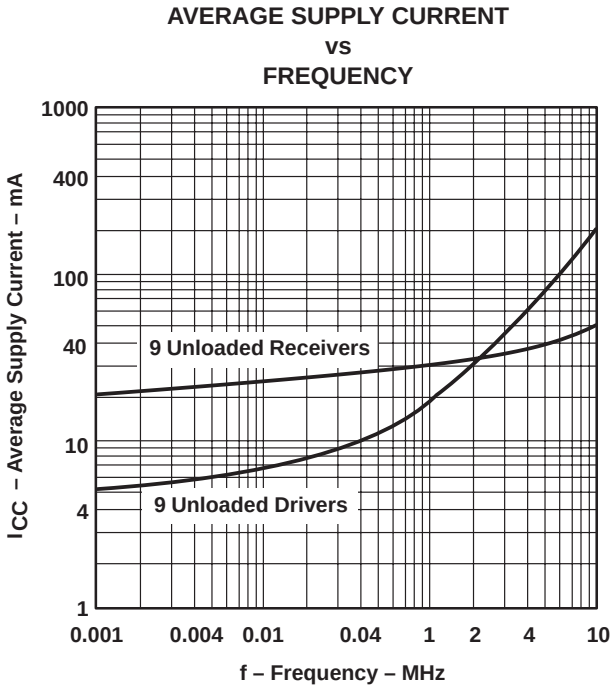



Figure 7

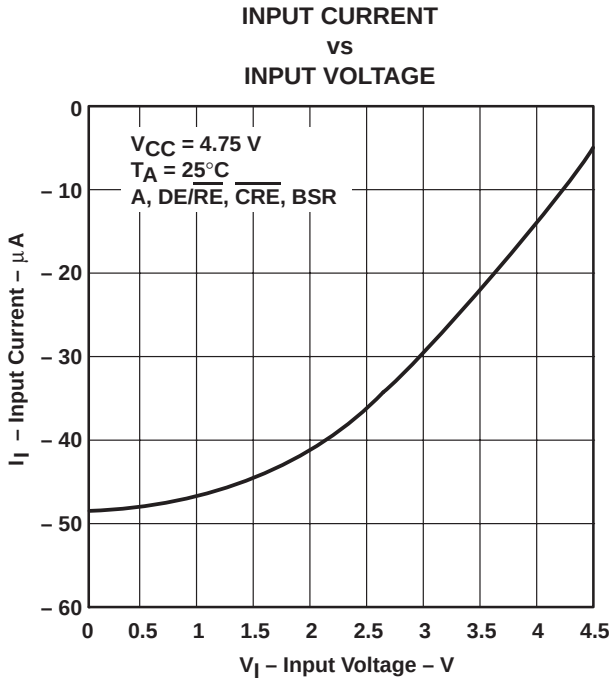



Figure 8

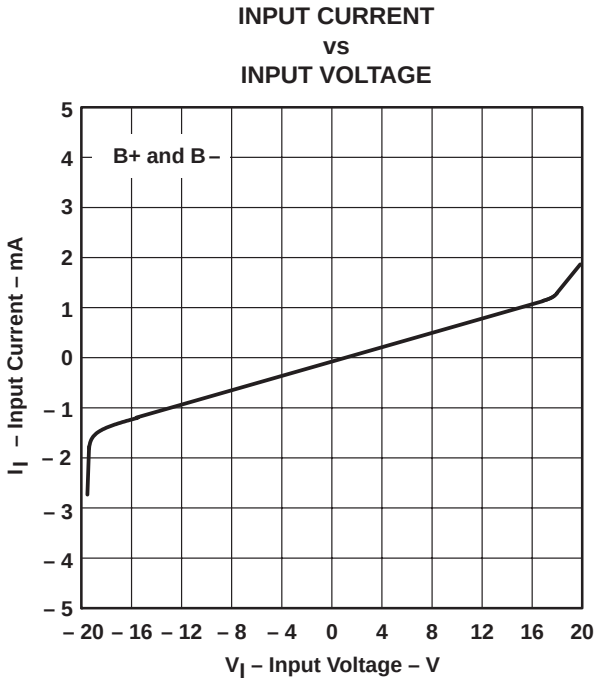



Figure 9

## TYPICAL CHARACTERISTICS

**DRIVER**
**LOW-LEVEL OUTPUT VOLTAGE**
**vs**
**LOW-LEVEL OUTPUT CURRENT**

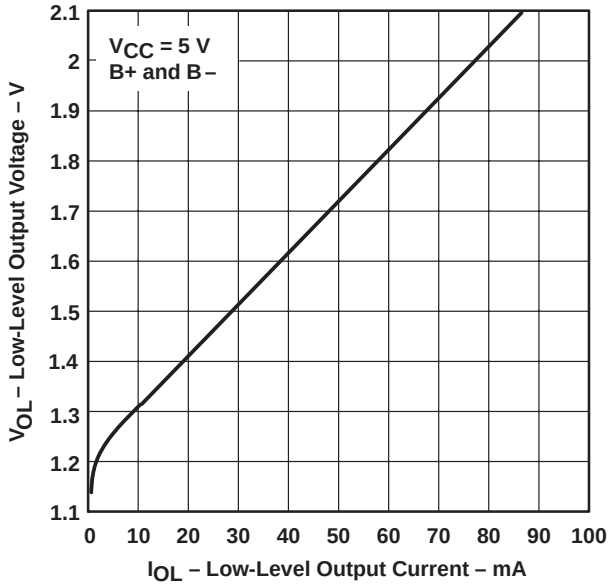



**Figure 10**

**DRIVER**
**HIGH-LEVEL OUTPUT VOLTAGE**
**vs**
**HIGH-LEVEL OUTPUT CURRENT**

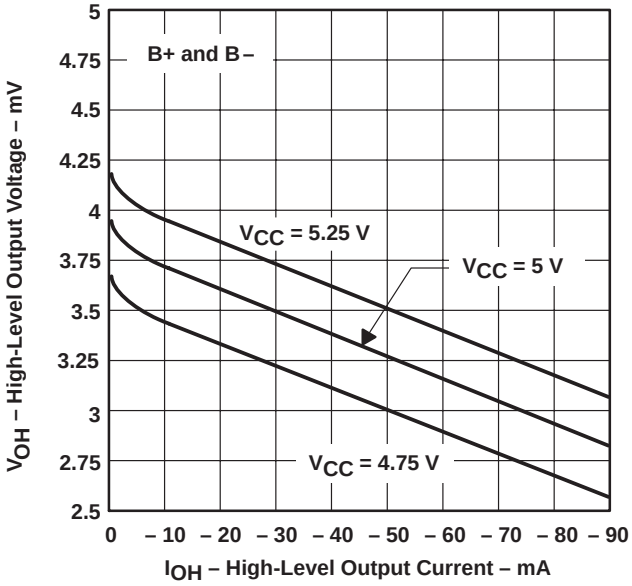



**Figure 11**

**DRIVER**
**DIFFERENTIAL OUTPUT VOLTAGE**
**vs**
**OUTPUT CURRENT**

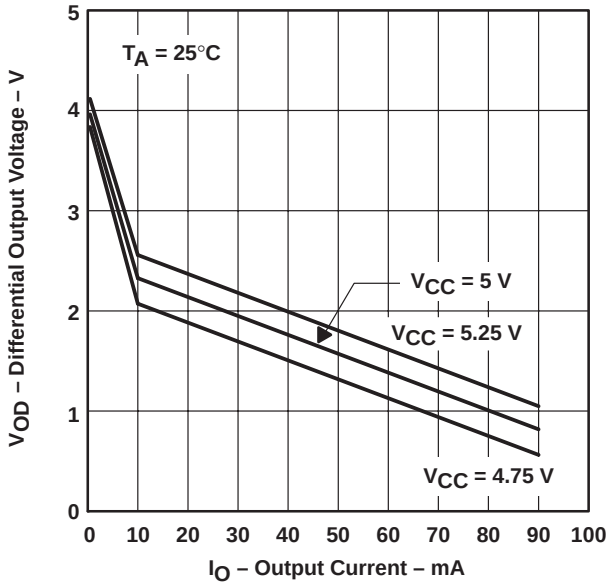



**Figure 12**

## TYPICAL CHARACTERISTICS

DRIVER
LOW-LEVEL OUTPUT CURRENT
vs
SUPPLY VOLTAGE

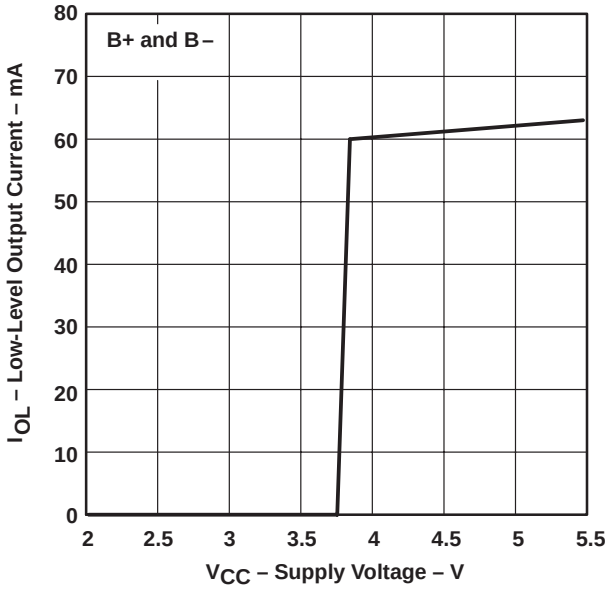



Figure 13

DRIVER
HIGH-LEVEL OUTPUT CURRENT
vs
SUPPLY VOLTAGE

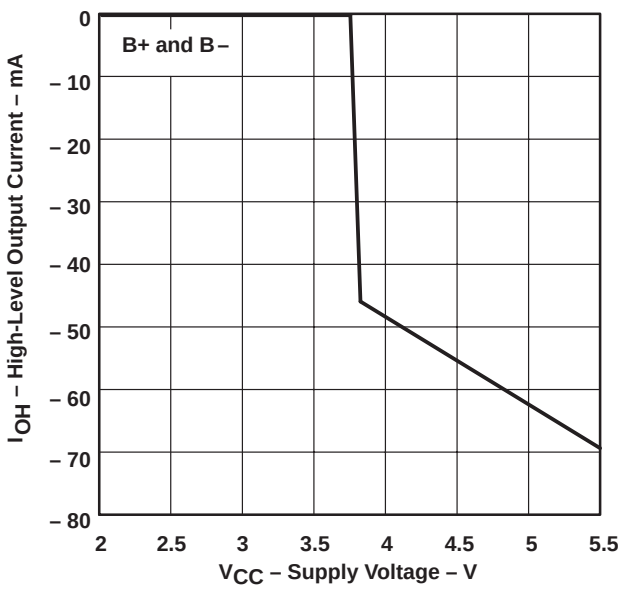



Figure 14

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

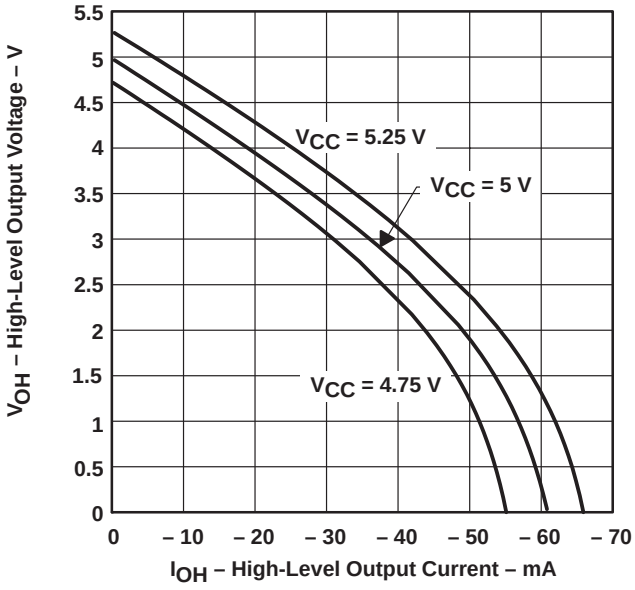



Figure 15

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

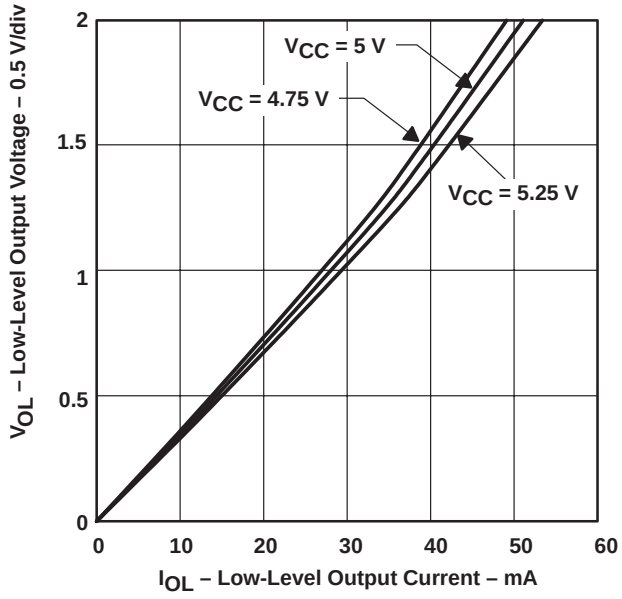



Figure 16

## TYPICAL CHARACTERISTICS

**DRIVER**
**DIFFERENTIAL OUTPUT VOLTAGE**
**vs**
**FREE-AIR TEMPERATURE**

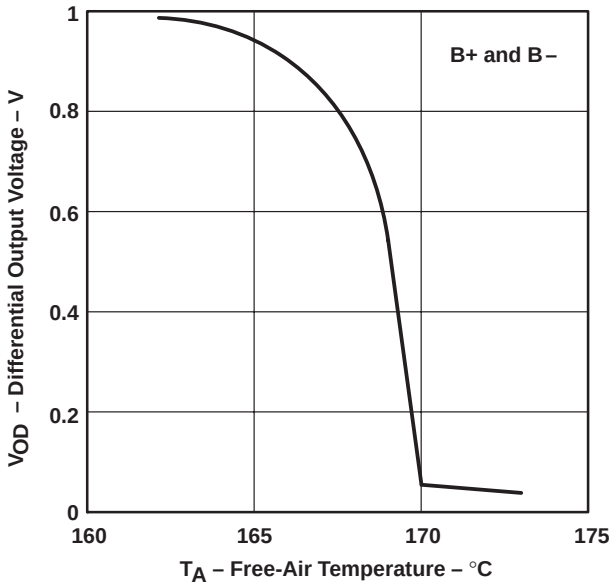



**Figure 17**

**RECEIVER**
**PROPAGATION DELAY TIME**
**vs**
**FREE-AIR TEMPERATURE**

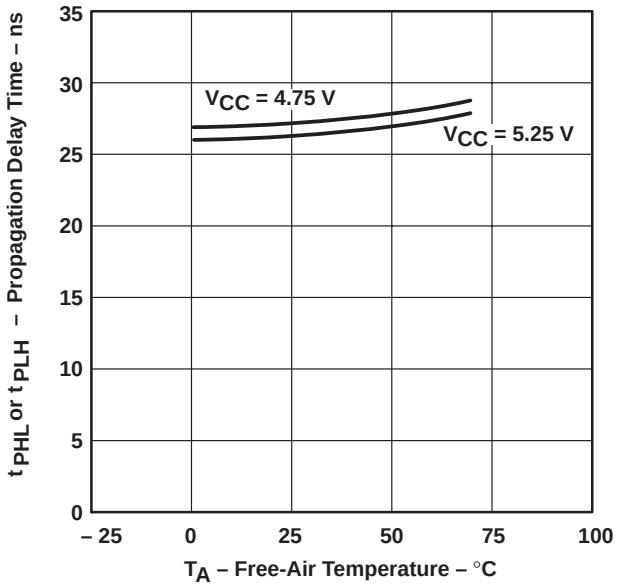



**Figure 18**

**DRIVER**
**PROPAGATION DELAY TIME**
**vs**
**FREE-AIR TEMPERATURE**

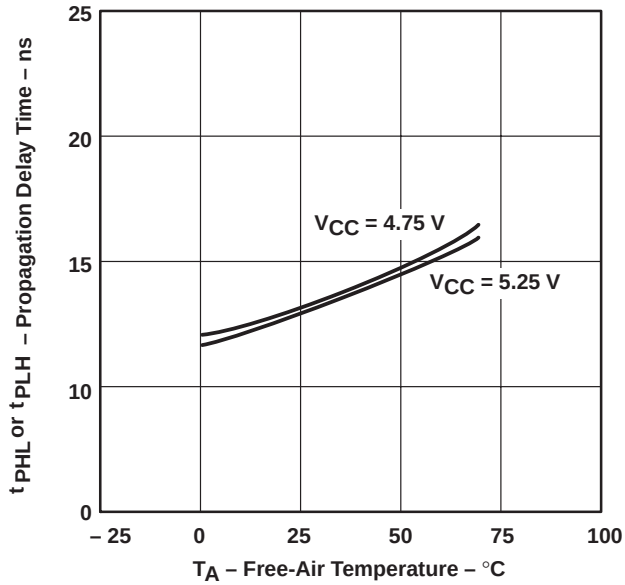



**Figure 19**

## APPLICATION INFORMATION

### Table 1. Typical Signal and Terminal Assignments

| SIGNAL | TERMINAL | SCSI DATA | SCSI CONTROL | IPI DATA | IPI CONTROL |
|---|---|---|---|---|---|
| CDE0 | 54 | DIFFSENSE | DIFFSENSE | $V_{CC}$ | $V_{CC}$ |
| CDE1 | 55 | GND | GND | XMTA, XMTB | GND |
| CDE2 | 56 | GND | GND | XMTA, XMTB | SLAVE/MASTER |
| BSR | 2 | GND | GND | GND, BSR | GND |
| $\overline{\text{CRE}}$ | 3 | GND | GND | GND | $V_{CC}$ |
| 1A | 4 | DB0, DB8 | ATN | AD7, BD7 | NOT USED |
| 1DE/$\overline{\text{RE}}$ | 5 | DBE0, DBE8 | INIT EN | GND | GND |
| 2A | 6 | DB1, DB9 | BSY | AD6, BD6 | NOT USED |
| 2DE/$\overline{\text{RE}}$ | 7 | DBE1, DBE9 | BSY EN | GND | GND |
| 3A | 8 | DB2, DB10 | ACK | AD5, BD5 | SYNC IN |
| 3DE/$\overline{\text{RE}}$ | 9 | DBE2, DBE10 | INIT EN | GND | GND |
| 4A | 10 | DB3, DB11 | RST | AD4, BD4 | SLAVE IN |
| 4DE/$\overline{\text{RE}}$ | 11 | DBE3, DBE11 | GND | GND | GND |
| 5A | 19 | DB4, DB12 | MSG | AD3, BD3 | NOT USED |
| 5DE/$\overline{\text{RE}}$ | 20 | DBE4, DBE12 | TARG EN | GND | GND |
| 6A | 21 | DB5, DB13 | SEL | AD2, BD2 | SYNC OUT |
| 6DE/$\overline{\text{RE}}$ | 22 | DBE5, DBE13 | SEL EN | GND | GND |
| 7A | 23 | DB6, DB14 | C/D | AD1, BD1 | MASTER OUT |
| 7DE/$\overline{\text{RE}}$ | 24 | DBE6, DBE14 | TARG EN | GND | GND |
| 8A | 25 | DB7, DB15 | REQ | AD0, BD0 | SELECT OUT |
| 8DE/$\overline{\text{RE}}$ | 26 | DBE7, DBE15 | TARG EN | GND | GND |
| 9A | 27 | DBP0, DBP1 | I/O | AP, BP | ATTENTION IN |
| 9DE/$\overline{\text{RE}}$ | 28 | DBPE0, DBPE1 | TARG EN | XMTA, XMTB | $V_{CC}$ |

ABBREVIATIONS:

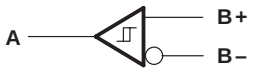
DBn, data bit n, where n = (0,1, . . . ,15)
DBEn, data bit n enable, where n = (0,1, . . . ,15)
DBP0, parity bit for data bits 0 through 7 or IPI bus A
DBPE0, parity bit enable for P0
DBP1, parity bit for data bits 8 through 15 or IPI bus B
DBPE1, parity bit enable for P1
ADn or BDn, IPI Bus A – Bit n (ADn) or Bus B – Bit n (BDn), where n = (0,1, . . . ,7)
AP or BP, IPI parity bit for bus A or bus B
XMTA or XMTB, transmit enable for IPI bus A or B
BSR, bit significant response
INIT EN, common enable for SCSI initiator mode
TARG EN, common enable for SCSI target mode

NOTE: Signal inputs are shown as active high. If only active-low inputs are available, logic inversion is accomplished by reversing the B+ and B– connecter terminal assignments.

## APPLICATION INFORMATION

### Function Tables

**RECEIVER**

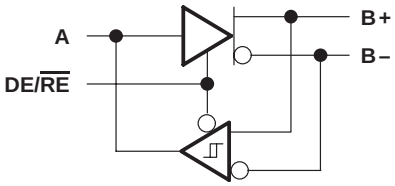



| INPUTS | | OUTPUT |
|---|---|---|
| B+† | B–† | A |
| L | H | L |
| H | L | H |

**DRIVER**

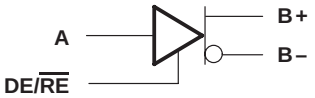
| INPUT | OUTPUTS | |
|---|---|---|
| A | B+ | B– |
| L | L | H |
| H | H | L |

**TRANSCEIVER**



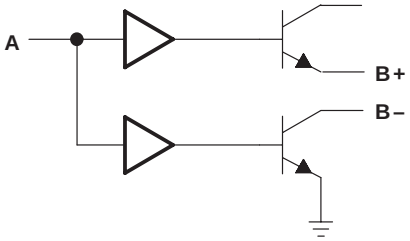

| INPUTS | | | | OUTPUTS | | |
|---|---|---|---|---|---|---|
| DE/$\overline{RE}$ | A | B+† | B–† | A | B+ | B– |
| L | – | L | H | L | – | – |
| L | – | H | L | H | – | – |
| H | L | – | – | – | L | H |
| H | H | – | – | – | H | L |

**DRIVER WITH ENABLE**



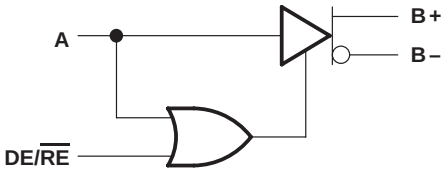

| INPUTS | | OUTPUTS | |
|---|---|---|---|
| DE/$\overline{RE}$ | A | B+ | B– |
| L | L | Z | Z |
| L | H | Z | Z |
| H | L | L | H |
| H | H | H | L |

**WIRED-OR DRIVER**




| INPUT | OUTPUTS | |
|---|---|---|
| A | B+ | B– |
| L | Z | Z |
| H | H | L |

**TWO-ENABLE INPUT DRIVER**

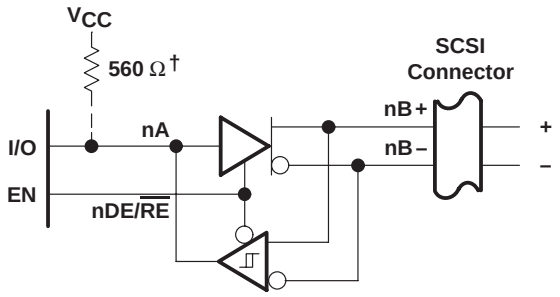



| INPUTS | | OUTPUTS | |
|---|---|---|---|
| DE/$\overline{RE}$ | A | B+ | B– |
| L | L | Z | Z |
| L | H | H | L |
| H | L | L | H |
| H | H | H | L |

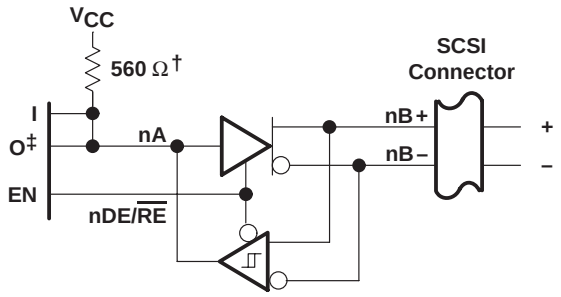
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

† An H in this column represents a voltage 200 mV higher than the other bus input. An L represents a voltage 200 mV lower than the other bus input. Any voltage less than 200 mV results in an indeterminate receiver output.

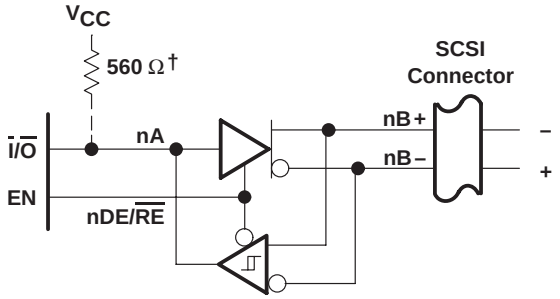
## APPLICATION INFORMATION



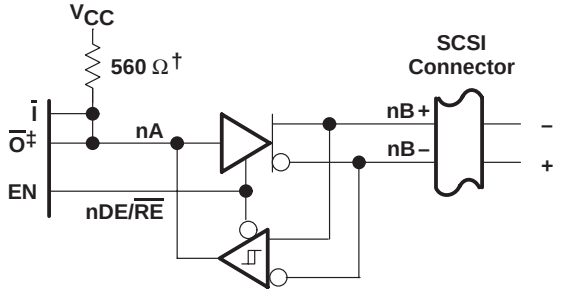

(a) ACTIVE-HIGH BIDIRECTIONAL I/O WITH SEPARATE ENABLE



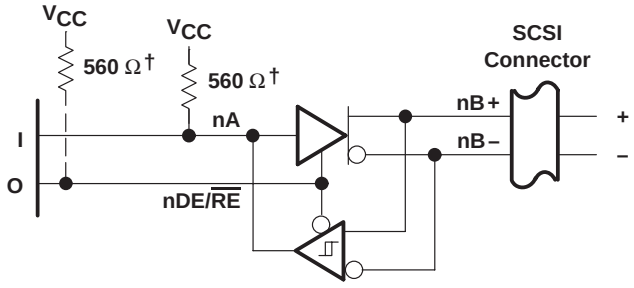

(d) SEPARATE ACTIVE-HIGH INPUT, OUTPUT, AND ENABLE



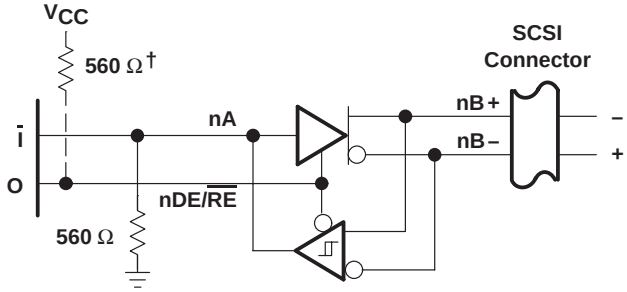

(b) ACTIVE-LOW BIDIRECTIONAL I/O WITH SEPARATE ENABLE




(e) SEPARATE ACTIVE-LOW INPUT AND OUTPUT AND ACTIVE-HIGH ENABLE




(c) WIRED-OR DRIVER AND ACTIVE-HIGH INPUT




(f) WIRED-OR DRIVER AND ACTIVE-LOW INPUT

† If 0, is open drain
‡ Must be open-drain or 3-state output
NOTE: The BSR, $\overline{CRE}$, A, and DE/$\overline{RE}$ inputs have internal pullups. CDE0, CDE1, and CDE2 have internal pulldowns.

**Figure 20. Typical SCSI Transceiver Connections**

## APPLICATION INFORMATION

### channel logic configurations with control input logic

The following logic diagrams show the positive-logic representation for all combinations of control inputs. The control inputs are from MSB to LSB; BSR, CDE0, CDE1, CDE2, and $\overline{\text{CRE}}$, and are shown below the diagrams. Channel 1 is at the top and channel 9 is at the bottom of the logic diagrams.

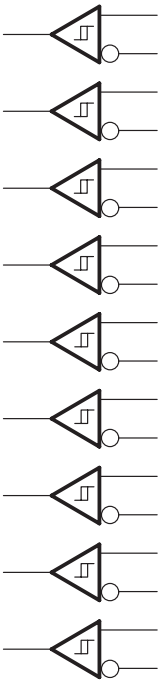


**Figure 21. 00000**

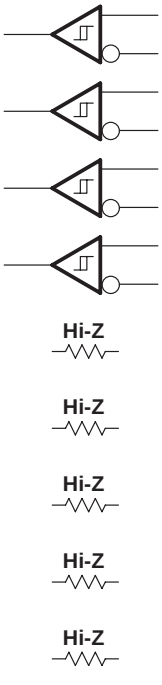



**Figure 22. 00001**

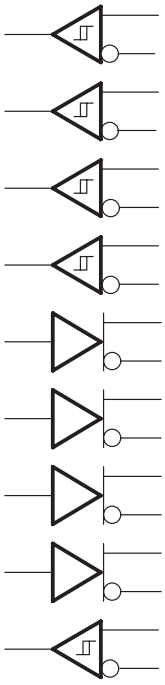


**Figure 23. 00010**

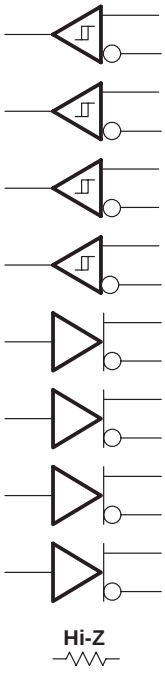



**Figure 24. 00011**

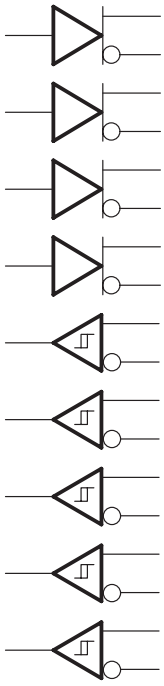


**Figure 25. 00100**

## APPLICATION INFORMATION

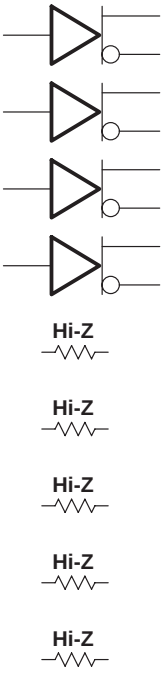



**Figure 26. 00101**

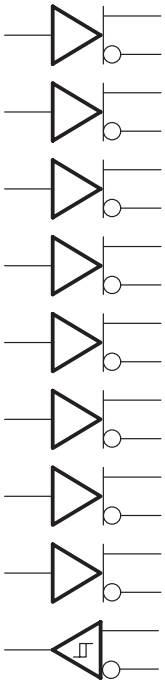


**Figure 27. 00110**

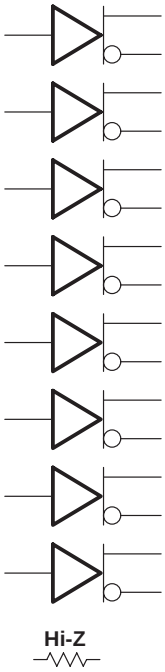



**Figure 28. 00111**

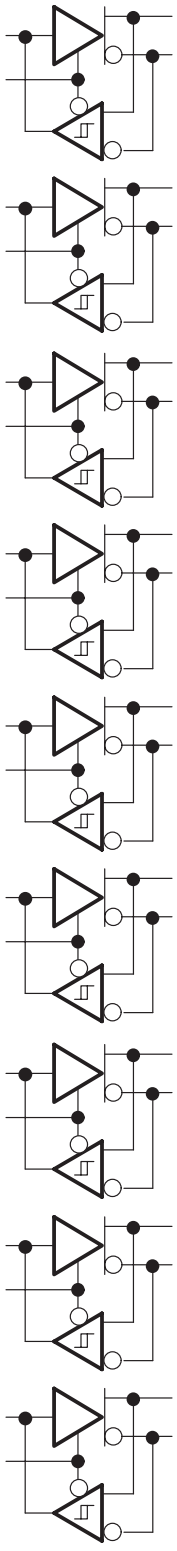


**Figure 29. 01000**

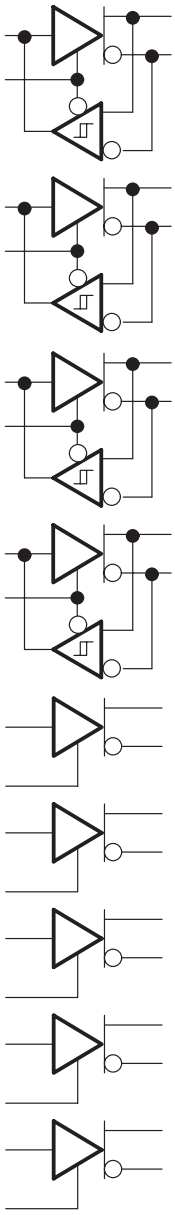


**Figure 30. 01001**

## APPLICATION INFORMATION

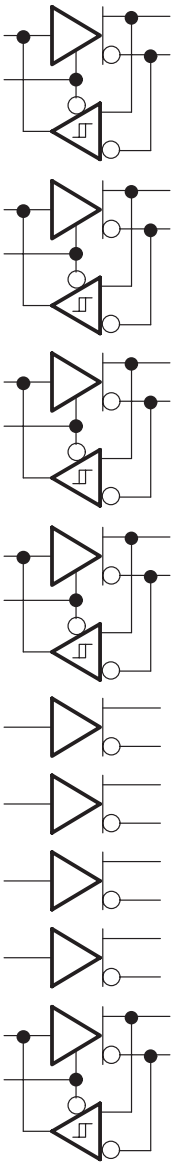


Figure 31. 01010

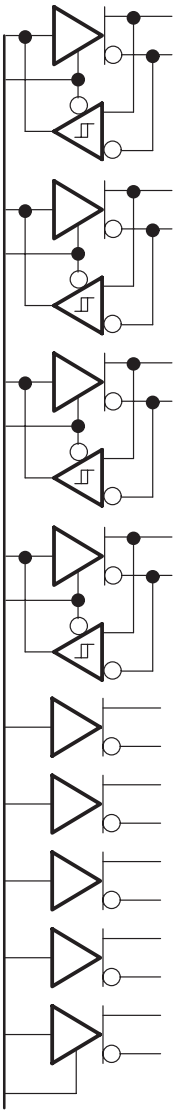


Figure 32. 01011

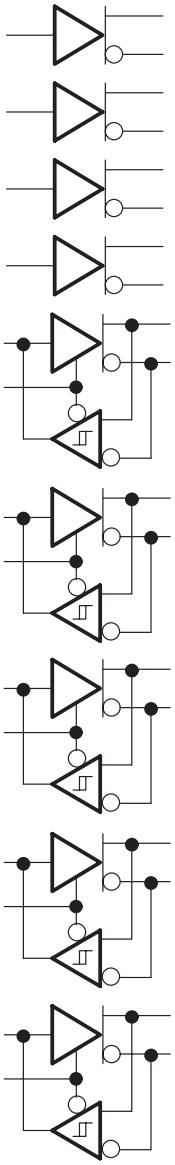


Figure 33. 01100

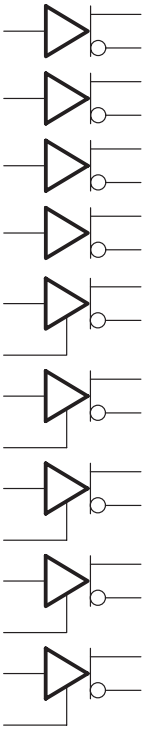


Figure 34. 01101

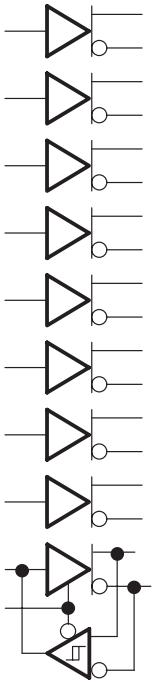


Figure 35. 01110

## APPLICATION INFORMATION

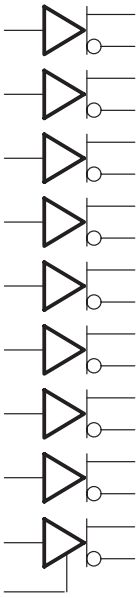


Figure 36. 01111

Figure 37. 10000 and 10001

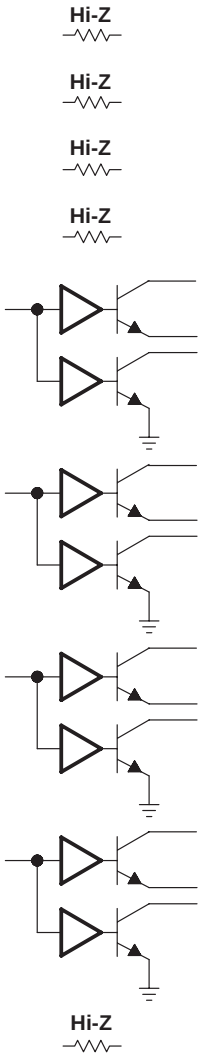



Figure 38. 10010 and 10011

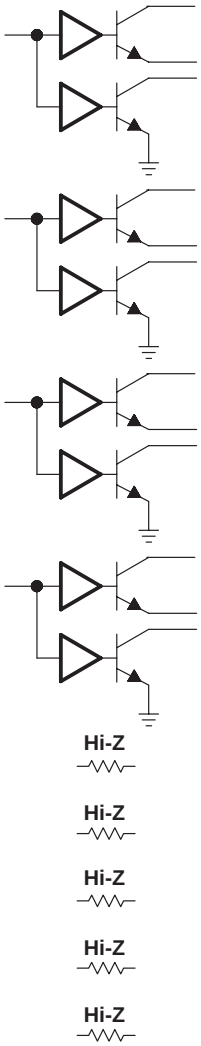



Figure 39. 10100 and 10101

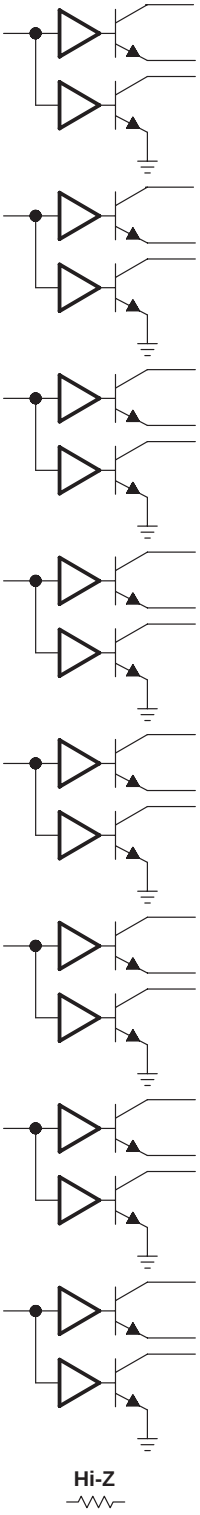



Figure 40. 10110 and 10111

## APPLICATION INFORMATION

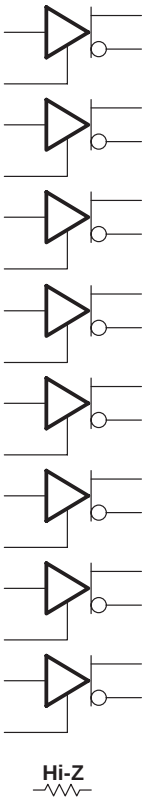



**Figure 41. 11000 and 11001**

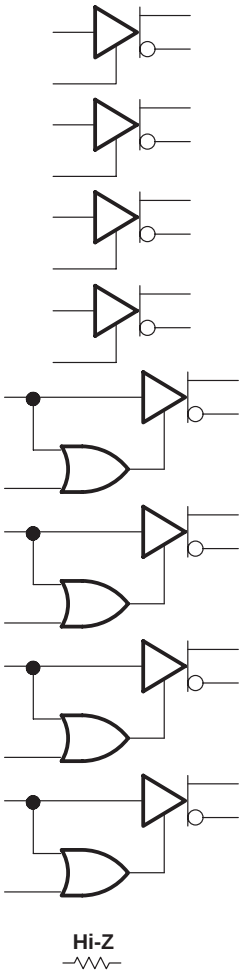



**Figure 42. 11010 and 11011**

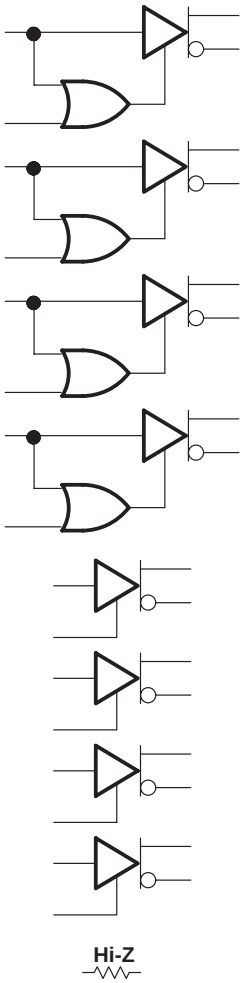



**Figure 43. 11100 and 11101**

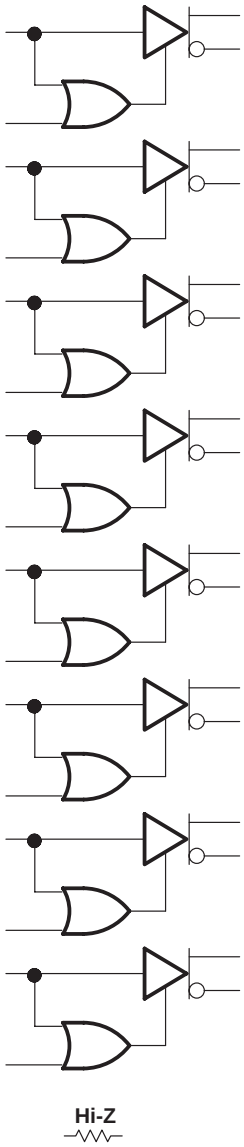



**Figure 44. 11110 and 11111**

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