National Semiconductor

August 2000

LMC6572/LMC6574 Dual and Quad Low Voltage (2.7V and 3V) Operational Amplifier

General Description

Low voltage operation and low power dissipation make the LMC6574/2 ideal for battery-powered systems.

3V amplifier performance is backed by 2.7V guarantees to ensure operation throughout battery lifetime. These guarantees also enable analog circuits to operate from the same 3.3V supply used for digital logic.

Battery life is maximized because each amplifier dissipates only micro-watts of power.

The LMC6574/2 does not sacrifice functionality for low voltage operation. The LMC6574/2 generates 120 dB of open-loop gain just like a conventional amplifier, but the LMC6574/2 can do this from a 2.7V supply.

These amplifiers are designed with features that optimize low voltage operation. The output voltage swings rail-to-rail to maximize signal-to-noise ratio and dynamic signal range. The common-mode input voltage range extends from 800 mV below the positive supply to 100 mV below ground.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

LMC6572 is also available in MSOP package which is almost half the size of a SO-8 device.

Features

(Typical unless otherwise noted)

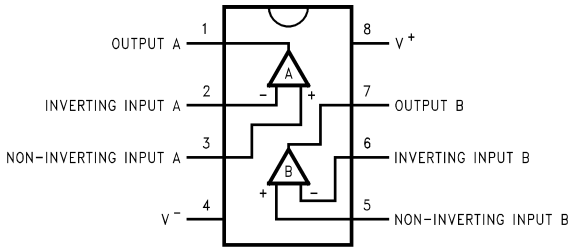
- Guaranteed 2.7V and 3V Performance
- Rail-to-Rail Output Swing (within 5 mV of supply rail, 100 kΩ load)
- Ultra-Low Supply Current: 40 µA/Amplifier
- Low Cost
- Ultra-Low Input Current: 20 fA
- High Voltage Gain @ V_S=2.7V, R_L=100 kΩ: 120 dB
- Specified for 100 kΩ and 5 kΩ loads
- Available in MSOP Package

Applications

- Transducer Amplifier
- Portable or Remote Equipment
- Battery-Operated Instruments
- Data Acquisition Systems
- Medical Instrumentation
- Improved Replacement for TLV2322 and TLV2324

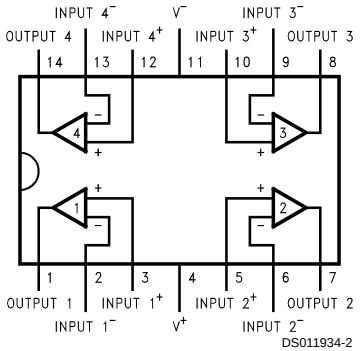
Connection Diagrams

8-Pin DIP/SO/MSOP



Order Number LMC6572AIN, LMC6572BIN, LMC6572AIM, LMC6572AIMX, LMC6572BIM, LMC6572BIMX, LMC6572BIMM or LMC6572BIMMX
See NS Package Number N08E, M08A or MUA08A

14-Pin DIP/SO



Order Number LMC6574AIN, LMC6574BIN, LMC6574AIM, LMC6574AIMX, LMC6574BIM or LMC6574BIMX
See NS Package Number N14A or M14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	2000V
Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) +0.3V, (V^-) −0.3V
Supply Voltage $(V^+ - V^-)$	12V
Current at Input Pin	±5 mA
Current at Output Pin (Note 3)	±10 mA
Current at Power Supply Pin	35 mA
Lead Temperature (Soldering, 10 Seconds)	260˚C
Storage Temperature Range	−65˚C to +150˚C
Junction Temperature (Note 4)	150˚C

Operating Ratings (Note 1)

Supply Voltage	$2.7V \le V^+ \le 11V$
Junction Temperature Range	
LMC6572AI, LMC6572BI	$-40˚C \le T_J \le +85˚C$
LMC6574AI, LMC6574BI	$-40˚C \le T_J \le +85˚C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	115˚C/W
M Package, 8-Pin Surface Mount	193˚C/W
MSOP Package, 8-Pin Mini SO	217˚C/W
N Package, 14-Pin Molded DIP	81˚C/W
M Package, 14-Pin Surface Mount	126˚C/W

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 2.7V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and $R_L > 1M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6574AI LMC6572AI Limit (Note 6)	LMC6574BI LMC6572BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	V^+ = 2.7V and 3V		0.5	3	7	mV
					3.5	**7.5**	Max
TCV_{OS}	Input Offset Voltage Average Drift			1.5			µV/˚C
I_B	Input Current			0.02			pA
					10	**10**	Max
I_{OS}	Input Offset Current			0.01			pA
					6	**6**	Max
R_{IN}	Input Resistance			>1			Tera Ω
C_{IN}	Common-Mode Input Capacitance			3			pF
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 3.5V$ $V^+ = 5V$		75	63	60	dB
					60	**57**	Min
+PSRR	Positive Power Supply Rejection Ratio	$2.7V \le V^+ \le 5V$, $V^- = 0V$		75	67	60	dB
					65	**58**	Min
−PSRR	Negative Power Supply Rejection Ratio	$-2.7V \le V^- \le -5V$, $V^+ = 0V$		83	75	67	dB
					73	**65**	Min
V_{CM}	Input Common-Mode Voltage Range	V^+ = 2.7V and 3V for CMRR ≥ 50 dB		−0.1	−0.05	−0.05	V
					0	**0**	Max
				$V^+ - 0.8$	$V^+ - 1.0$	$V^+ - 1.0$	V
					$V^+ - 1.3$	**$V^+ - 1.3$**	Min
A_V	Large Signal Voltage Gain	R_L = 100 kΩ (Note 7)	Sourcing	1000			V/mV
			Sinking	500			V/mV

2.7V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 2.7V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and $R_L > 1M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6574AI LMC6572AI Limit (Note 6)	LMC6574BI LMC6572BI Limit (Note 6)	Units
V_O	Output Swing	V^+ = 2.7V	2.695	2.68	2.65	V
		R_L = 100 kΩ to $V^+/2$		**2.66**	**2.62**	Min
			0.005	0.03	0.06	V
				0.05	**0.09**	Max
		V^+ = 2.7V	2.66	2.55	2.45	V
		R_L = 5 kΩ to $V^+/2$		**2.45**	**2.35**	Min
			0.04	0.15	0.25	V
				0.25	**0.35**	Max
		V^+ = 3V	2.995	2.98	2.95	V
		R_L = 100 kΩ to $V^+/2$		**2.96**	**2.93**	Min
			0.005	0.03	0.06	V
				0.05	**0.09**	Max
		V^+ = 3V	2.96	2.85	2.75	V
		R_L = 5 kΩ to $V^+/2$		**2.75**	**2.65**	Min
			0.04	0.15	0.25	V
				0.25	**0.35**	Max
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V	6.0	4.0	3.0	mA
				3.0	**2.0**	Min
		Sinking, V_O = 2.7V	4.0	3.0	2.5	mA
				2.0	**1.5**	Min
I_S	Supply Current	Quad Package	160	240	240	µA
		V^+ = +2.7V, $V_O = V^+/2$		**280**	**280**	Max
		Quad Package	160	240	240	µA
		V^+ = +3V, $V_O = V^+/2$		**280**	**280**	Max
		Dual Package	80	120	120	µA
		V^+ = +2.7V, $V_O = V^+/2$		**140**	**140**	Max
		Dual Package	80	120	120	µA
		V^+ = +3V, $V_O = V^+/2$		**140**	**140**	Max

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 2.7V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and $R_L > 1$ MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6574AI LMC6572AI Limit (Note 6)	LMC6574BI LMC6572BI Limit (Note 6)	Units
SR	Slew Rate	V^+ = 2.7V and 3V	90	30	30	V/ms
		(Note 8)		**10**	**10**	Min
GBW	Gain-Bandwidth Product	V^+ = 3V	0.22			MHz
ϕ_m	Phase Margin		60			Deg
G_m	Gain Margin		12			dB
	Amp-to-Amp Isolation	(Note 9)	120			dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	45			$nV/\sqrt{Hz}$
		V_{CM} = 1V				
i_n	Input-Referred	F = 1 kHz	0.002			$pA/\sqrt{Hz}$

2.7V AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = V^+/2 and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6574AI LMC6572AI Limit (Note 6)	LMC6574BI LMC6572BI Limit (Note 6)	Units
	Current Noise					
T.H.D.	Total Harmonic Distortion	F = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 1.0 V_{PP}	0.05			%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C.

Note 4: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

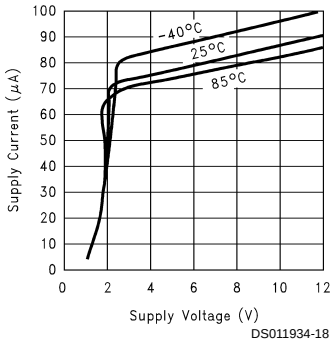
Note 7: V^+ = 3V, V_{CM} = 1.5V and R_L connected to 1.5V. For Sourcing tests, 1.5V ≤ V_O ≤ 2.5V. For Sinking tests, 0.5V ≤ V_O ≤ 1.5V.

Note 8: Connected as Voltage Follower with 1.0V step input. Number specified is the slower of the positive and negative slew rates.

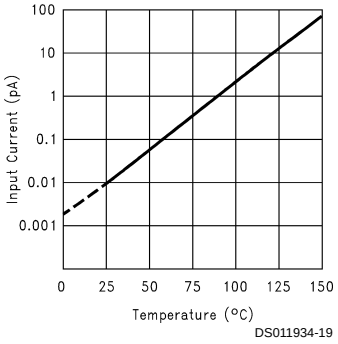
Note 9: Input referred, V^+ = 3V and R_L = 100 kΩ connected to 1.5V. Each amp excited in turn with 1 KHz to produce V_O = 2 V_{PP}.

Typical Performance Characteristics V_S = +3V, T_A = 25˚C, Unless otherwise specified

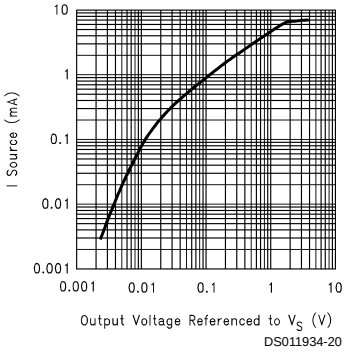
Supply Current vs Supply Voltage (Dual Package)



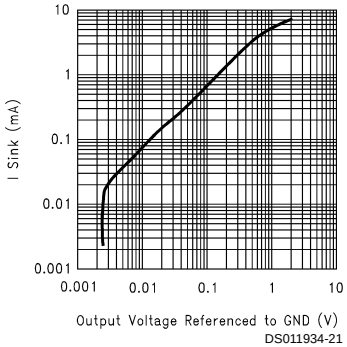
Input Current vs Temperature



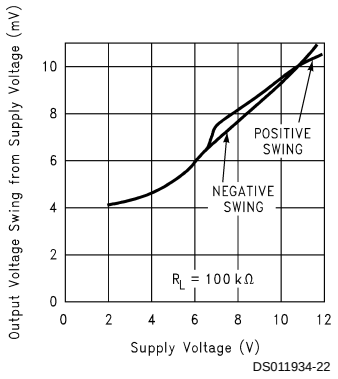
Sourcing Current vs Output Voltage



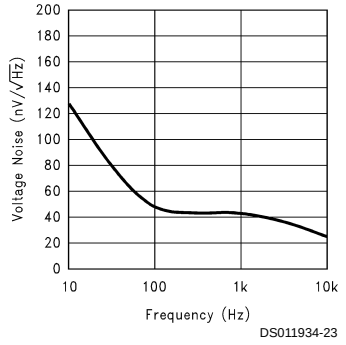
Sinking Current vs Output Voltage



Output Voltage Swing vs Supply Voltage

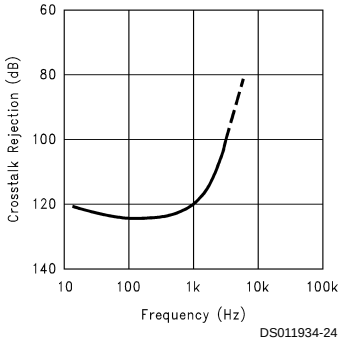


Input Voltage Noise vs Frequency



Typical Performance Characteristics V_S = +3V, T_A = 25˚C, Unless otherwise specified (Continued)

Crosstalk Rejection vs Frequency



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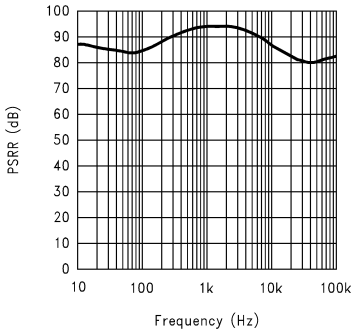
Positive PSRR vs Frequency



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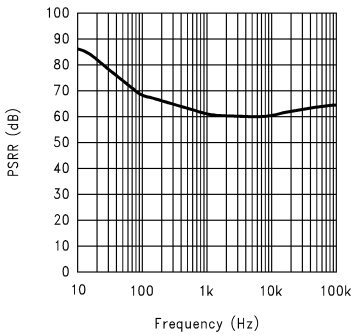
Negative PSRR vs Frequency



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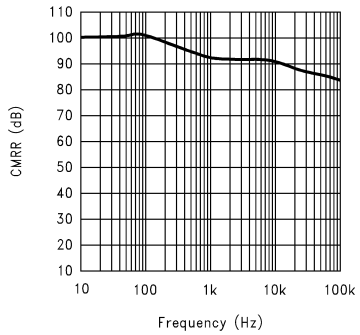
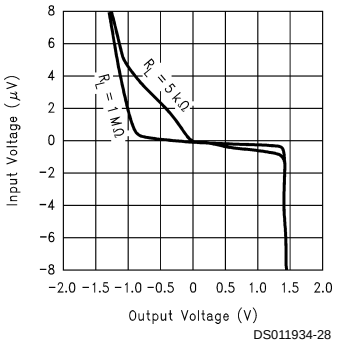
CMRR vs Frequency



DS011934-27

Input Voltage vs Output Voltage (V_S = ±1.5)



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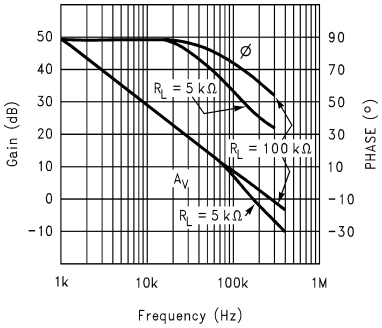
Open Loop Frequency Response



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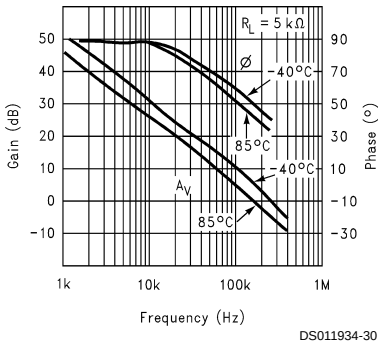
Open Loop Frequency Response vs Temperature



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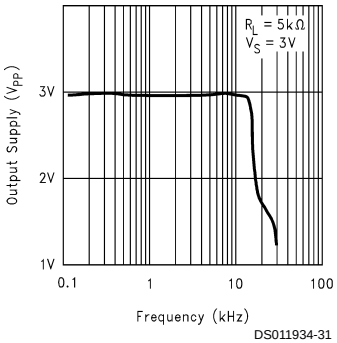
Maximum Output Swing vs Frequency



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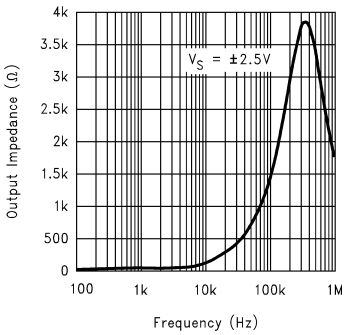
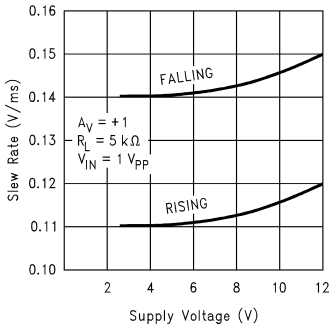
Z_{OUT} vs Frequency



DS011934-32

Typical Performance Characteristics V_S = +3V, T_A = 25˚C, Unless otherwise specified (Continued)

Slew Rate vs Supply Voltage



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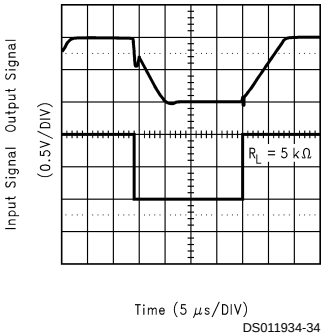
Non-Inverting Large Signal Pulse Response



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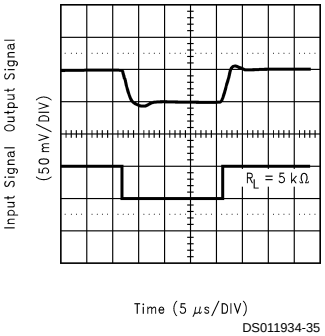
Non-Inverting Small Signal Pulse Response



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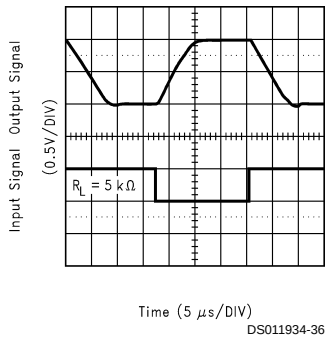
Inverting Large Signal Pulse Response



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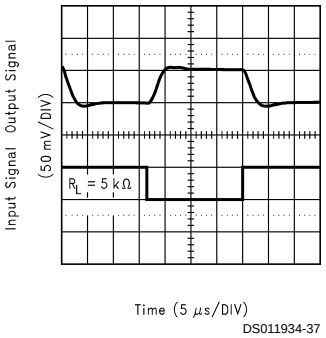
Inverting Small Signal Pulse Response



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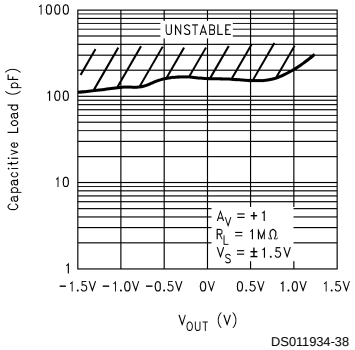
Stability vs Capacitive Load



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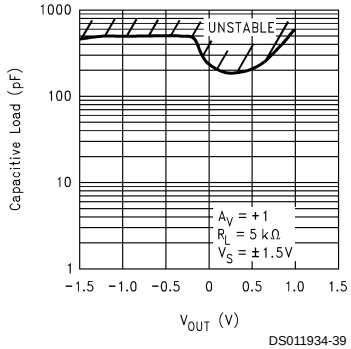
Stability vs Capacitive Load



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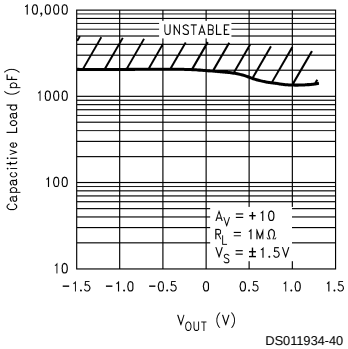
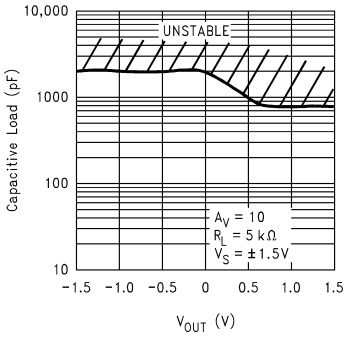
Stability vs Capacitive Load



DS011934-40

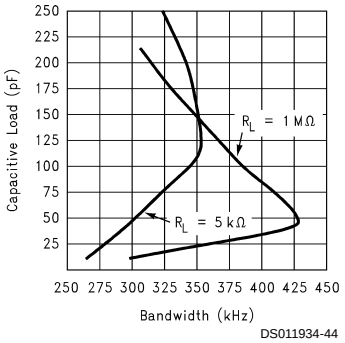
Stability vs Capacitive Load



DS011934-41

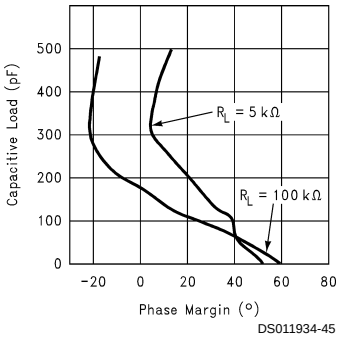
Typical Performance Characteristics V_S = +3V, T_A = 25°C, Unless otherwise specified (Continued)

Bandwidth vs Capacitive Load



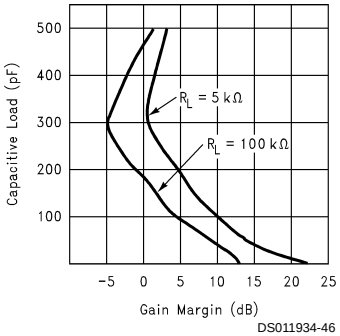
DS011934-44

Capacitive Load vs Phase Margin



DS011934-45

Capacitive Load vs Gain Margin



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Applications Hints

1.0 LOW VOLTAGE AMPLIFIER TOPOLOGY

The LMC6574/2 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6574/2 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

2.0 COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6574/2.

Although the LMC6574/2 is highly stable over a wide range of operating conditions, a large feedback resistor will react even with small values of capacitance at the input of the op-amp to reduce phase margin. The capacitance at the input of the op-amp comes from transducers, photodiodes and circuit board parasitics.

The effect of input capacitance can be compensated for by adding a capacitor, C_f, around the feedback resistors (as in *Figure 1*) such that:

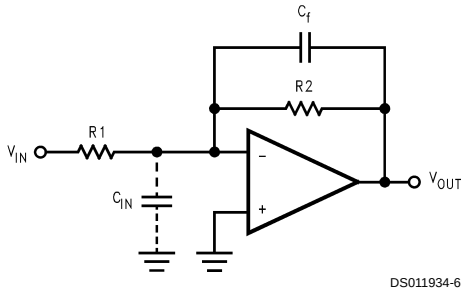
$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1\, C_{IN} \leq R_2\, C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.

When high input impedances are demanded, guarding of the LMC6574/2 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See *Printed-Circuit-Board Layout for High Impedance Work).*

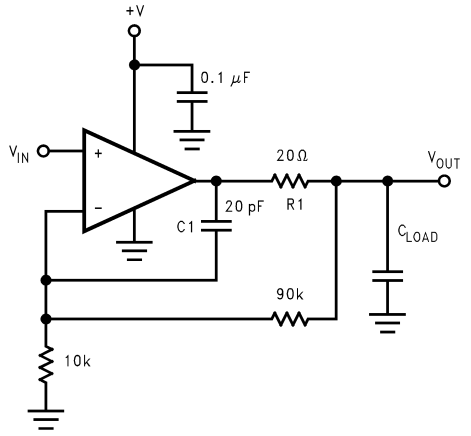


DS011934-6

FIGURE 1. Cancelling the Effect of Input Capacitance

3.0 CAPACITIVE LOAD TOLERANCE

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2*.



DS011934-7

FIGURE 2. LMC6574/2 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2*, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency compo-

Applications Hints (Continued)

nent of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

4.0 PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6574/2, typically less than 20 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6574/2's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 250 times degradation from the LMC6574/2's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figure 4* for typical connections of guard rings for standard op-amp configurations.

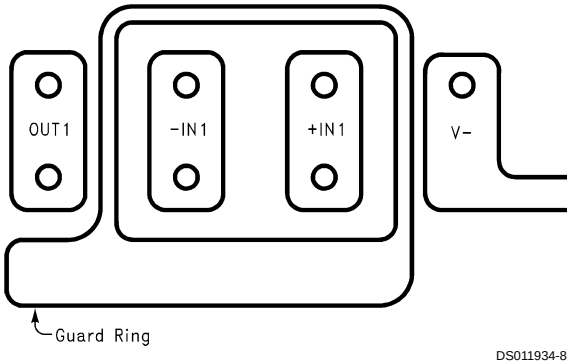


FIGURE 3. Example of Guard Ring in P.C. Board Layout

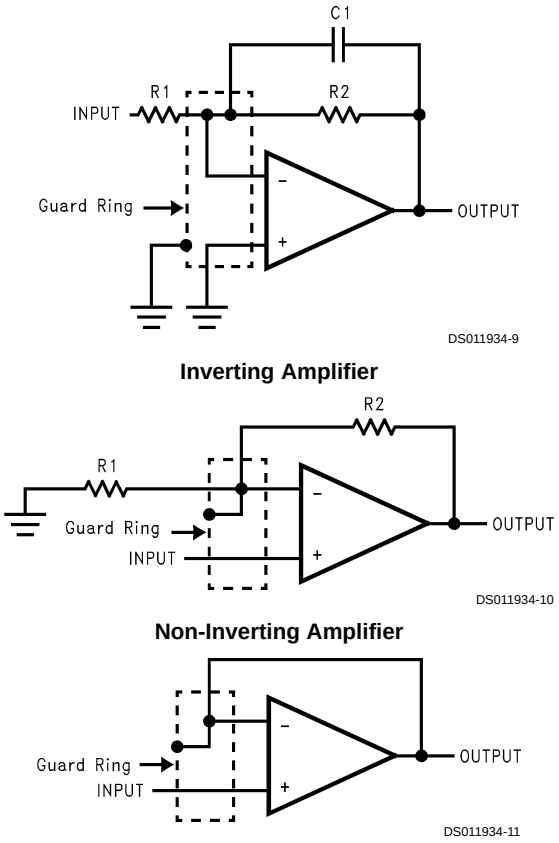
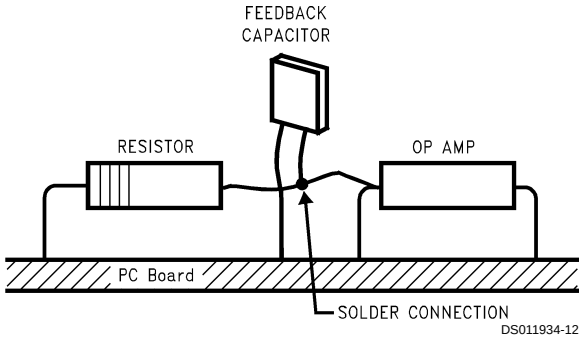


FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

FIGURE 5. Air Wiring

Applications Hints (Continued)

5.0 SPICE MACROMODEL

A spice macromodel is available for the LMC6574/2. This model includes accurate simulation of:

- input common-mode voltage range
- frequency and transient response
- GBW dependence on loading conditions
- quiescent and dynamic supply current
- output swing dependence on loading conditions

and many more characteristics as listed on the macromodel disk.

Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.

Typical Single-Supply Applications

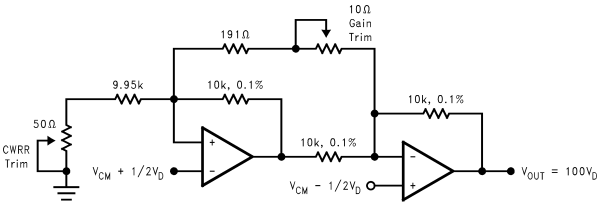


FIGURE 6. Low-Power Two-Op-Amp Instrumentation Amplifier

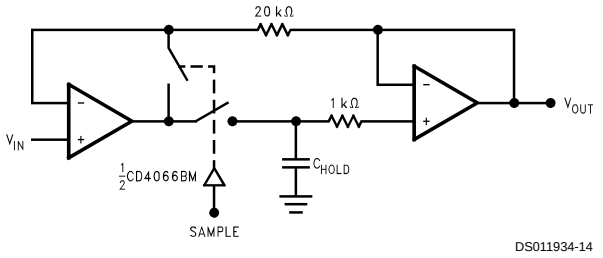


FIGURE 7. Sample and Hold

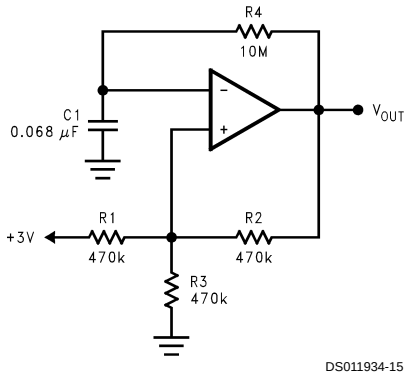


FIGURE 8. 1 Hz Square Wave Oscillator

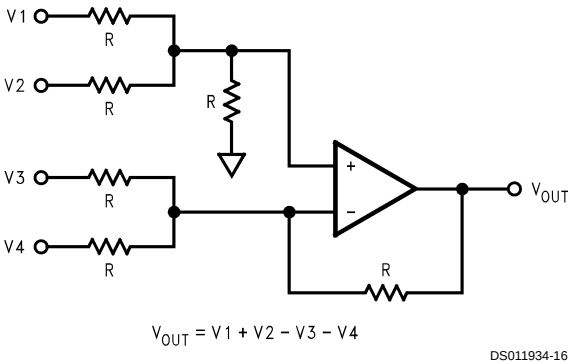


FIGURE 9. Adder/Subtractor Circuit

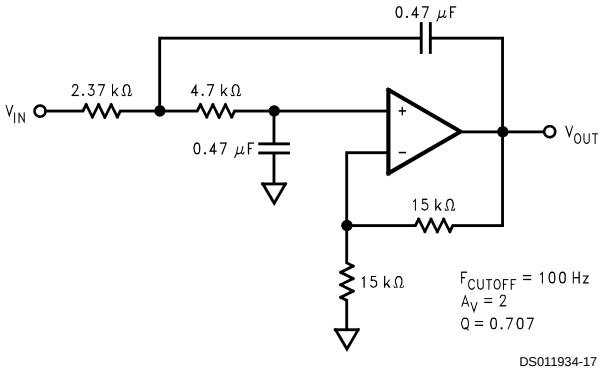
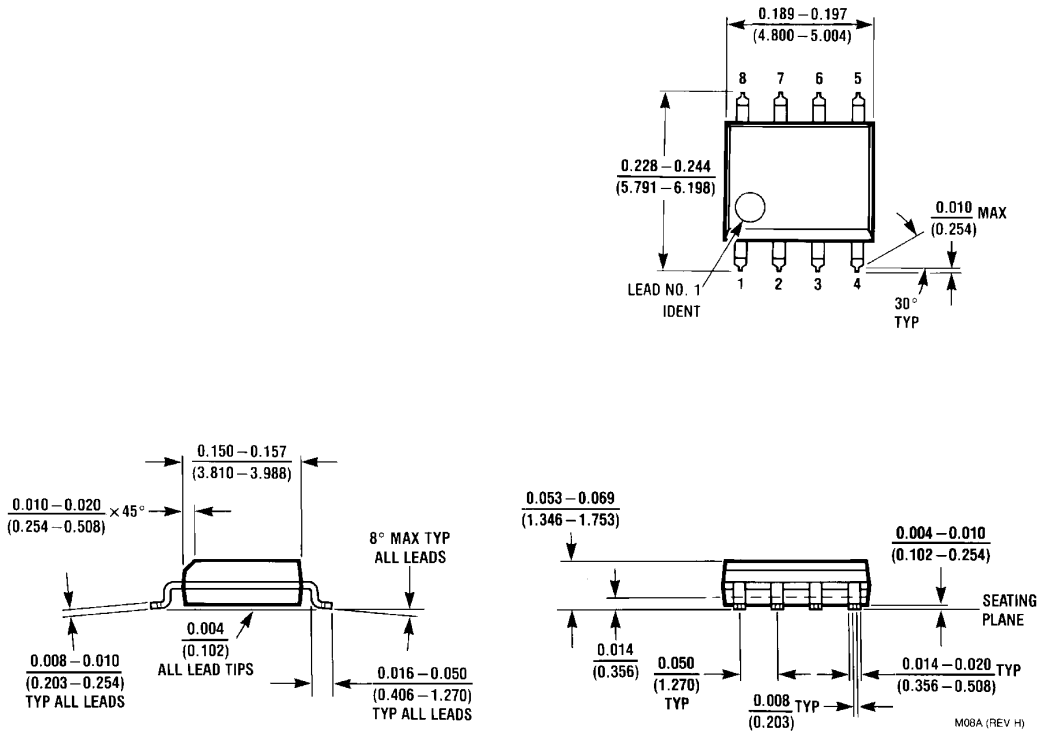


FIGURE 10. Low Pass Filter

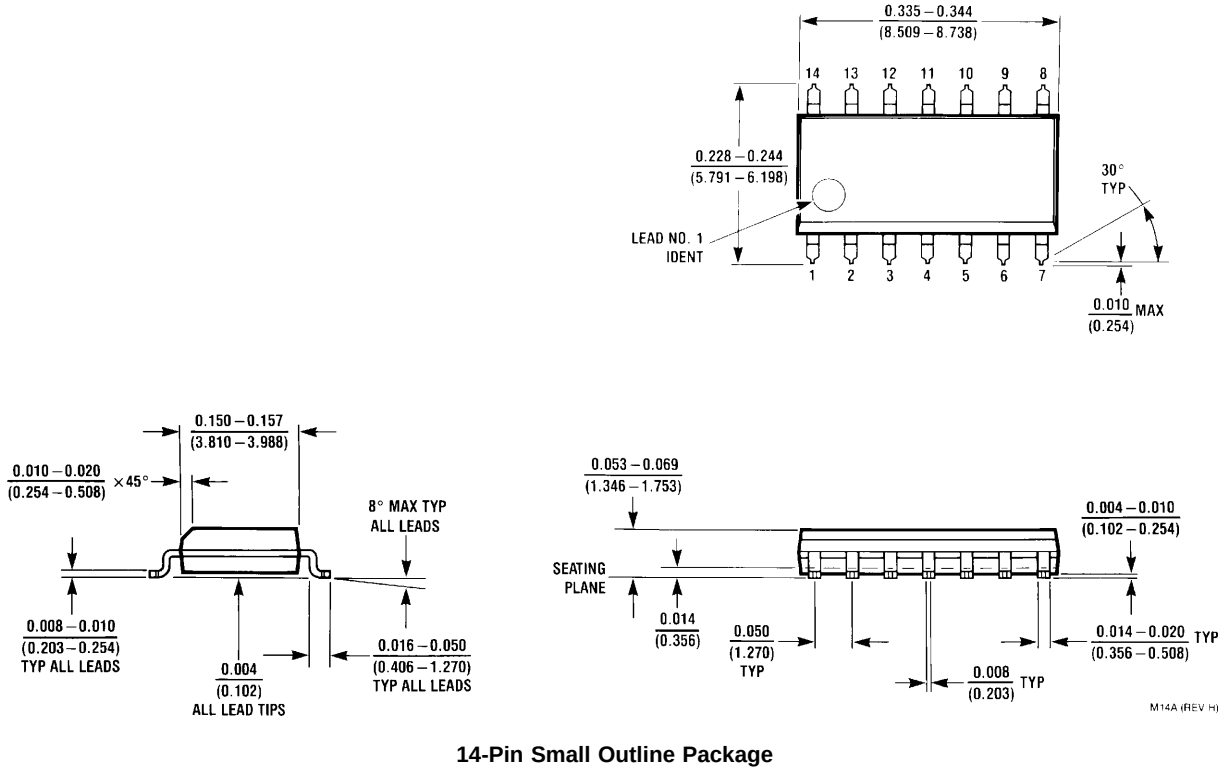
Ordering Information

Package	Temperature Range Industrial, −40˚C to +85˚C	NSC Drawing	Transport Media
8-Pin Molded DIP	LMC6572AIN, LMC6572BIN	N08E	Rail
8-Pin Small Outline	LMC6572AIM, LMC6572BIM	M08A	Rail
	LMC6572AIMX, LMC6572BIMX		Tape and Reel
8-Pin Mini SO	LMC6572BIMM	MUA08A	Rail
	LMC6572BIMMX		Tape and Reel
14-Pin Molded DIP	LMC6574AIN, LMC6574BIN	N14A	Rail
14-Pin Small Outline	LMC6574AIM, LMC6574BIM	M14A	Rail
	LMC6574AIMX, LMC6574BIMX		Tape and Reel

Physical Dimensions inches (millimeters) unless otherwise noted

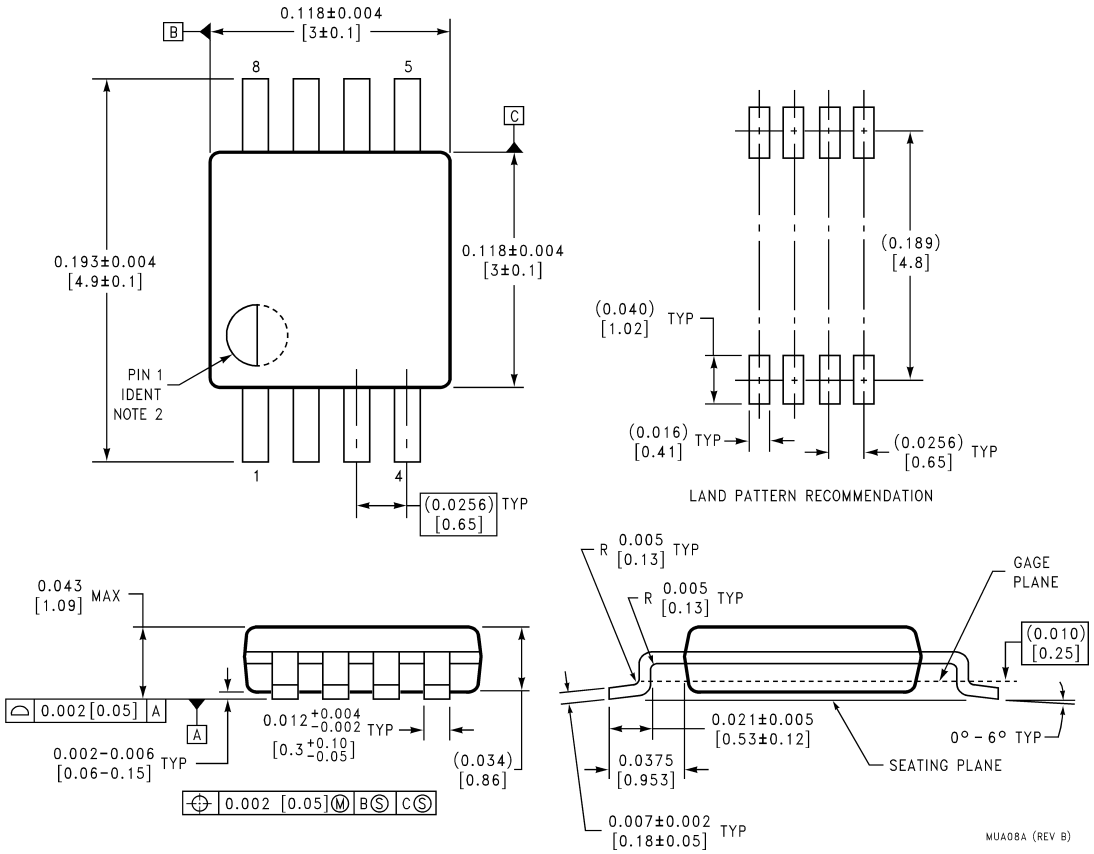


8-Pin Small Outline Package
Order Package Number LMC6572AIM, LMC6572AIMX, LMC6572BIM or LMC6572BIMX
NS Package Number M08A

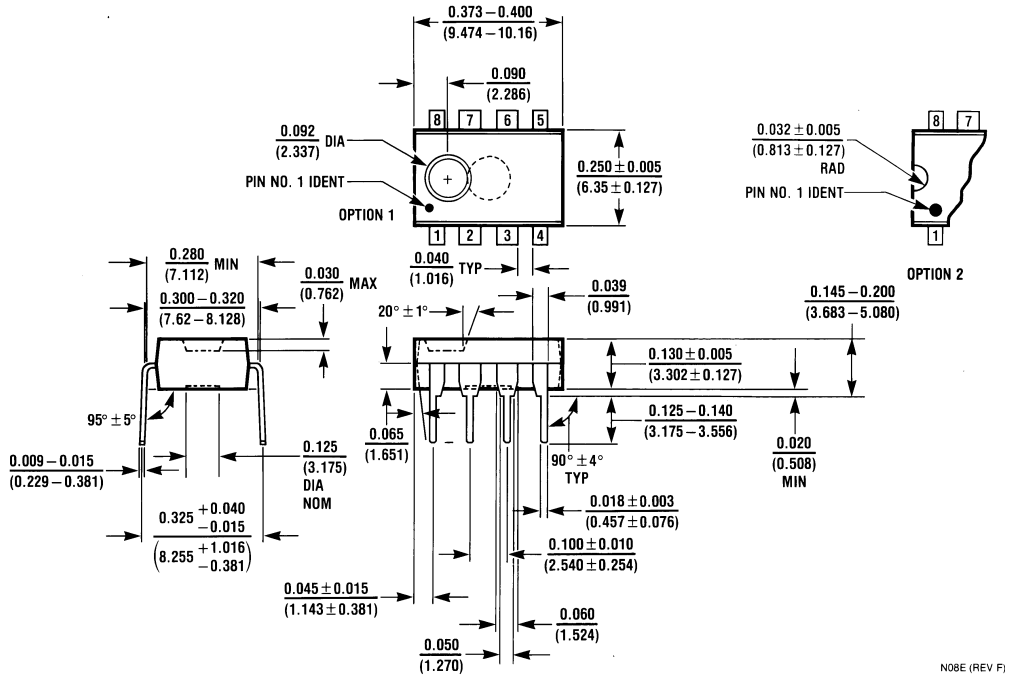


14-Pin Small Outline Package
Order Package Number LMC6574AIM, LMC6574AIMX, LMC6574BIM or LMC6574BIMX
NS Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

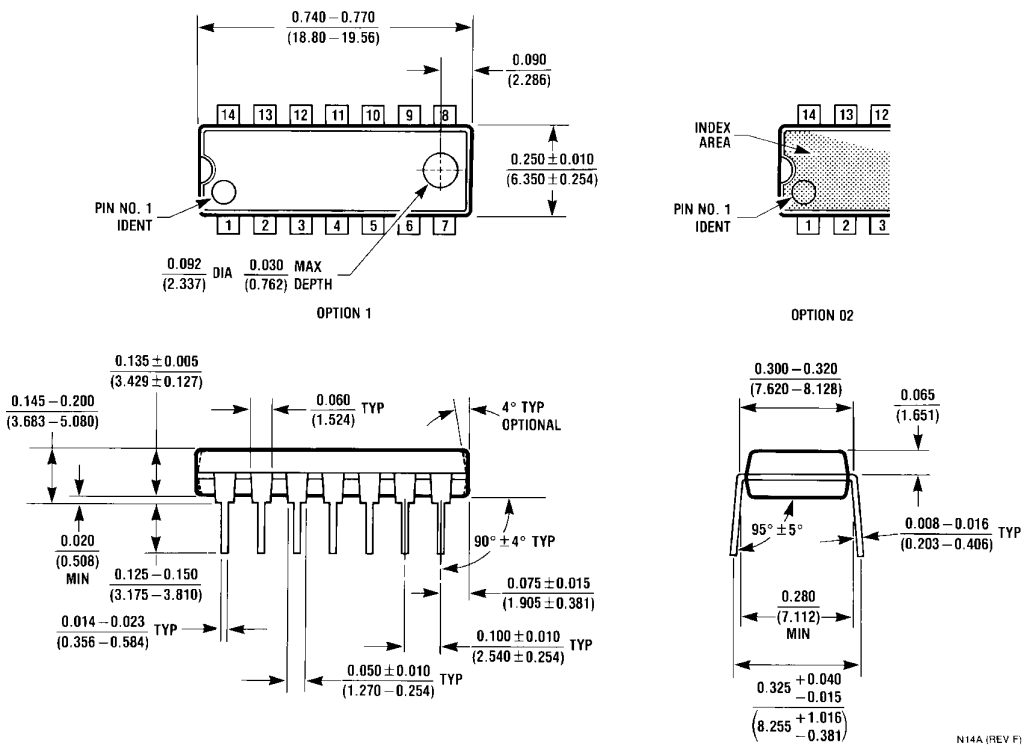


8-Lead Mini-Small Outline Molded Package, JEDEC
Order Number LMC6572BIMM or LMC6572BIMMX
NS Package Number MUA08A



8-Pin Molded Dual-In-Line Package
Order Number LMC6572AIN or LMC6572BIN
NS Package Number N08E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Pin Molded Dual-In-Line Package
Order Number LMC6574AIN or LMC6574BIN
NS Package Number N14A

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National Semiconductor Corporation
Americas
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Email: support@nsc.com
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National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
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National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

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