

1 MHz, Low-Power Op Amp

Features

- Available in 5-Lead SC-70 and 5-Lead SOT-23 Packages
- Gain Bandwidth Product: 1 MHz (typical)
- Rail-to-Rail Input/Output
- Supply Voltage: 1.8V to 6.0V
- Supply Current: I_Ω = 100 µA (typical)
- Phase Margin: 90° (typical)
- Temperature Range:
 - Industrial: -40°C to +85°C
 - Extended: -40°C to +125°C
- · Available in Single, Dual and Quad Packages

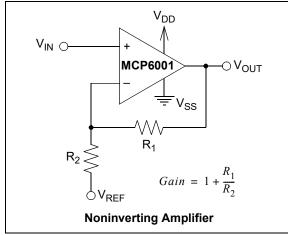
Applications

- · Automotive
- Portable Equipment
- Photodiode Amplifier
- Analog Filters
- Notebooks and PDAs
- Battery-Powered Systems

Design Aids

- · SPICE Macro Models
- FilterLab[®] Software
- Mindi[™] Circuit Designer and Analog Simulator
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

Typical Application

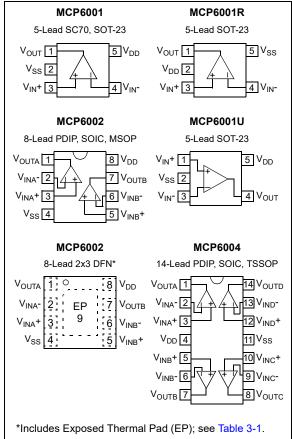


Description

The Microchip Technology Inc. MCP6001/2/4 family of operational amplifiers (op amps) is specifically designed for general purpose applications. This family has a 1 MHz Gain Bandwidth Product (GBWP) and 90° phase margin (typical). It also maintains a 45° phase margin (typical) with a 500 pF capacitive load. This family operates from a single-supply voltage as low as 1.8V, while drawing 100 μ A (typical) quiescent current. Additionally, the MCP6001/2/4 supports rail-to-rail input and output swing, with a Common-mode input voltage range of V_{DD} + 300 mV to V_{SS} – 300 mV. This family of op amps is designed with Microchip's advanced CMOS process.

The MCP6001/2/4 family is available in the industrial and extended temperature ranges, with a power supply range of 1.8V to 6.0V.

Package Types



NOTES:

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V _{DD} – V _{SS}
Current at Analog Input Pins (V _{IN} +, V _{IN} -)±2 mA
Analog Inputs (V _{IN} +, V _{IN} -) ⁺⁺ V _{SS} – 1.0V to V _{DD} + 1.0V
All Other Inputs and Outputs
Difference Input Voltage $ V_{DD} - V_{SS} $
Output Short-Circuit CurrentContinuous
Current at Output and Supply Pins±30 mA
Storage Temperature65°C to +150°C
Maximum Junction Temperature (T _J)+150°C
ESD Protection On All Pins (HBM; MM) \geq 4 kV; 200V

- **†** Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- **††** See Section 4.1.2 "Input Voltage and Current Limits".

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, $T_A = +25^{\circ}C$, $V_{DD} = +1.8V$ to +5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L and $V_{OUT} \approx V_{DD}/2$ (refer to Figure 1-1).

Parameters	Sym	Min	Тур	Max	Units	Conditions
Input Offset				•		-
Input Offset Voltage	V _{OS}	-4.5		+4.5	mV	V _{CM} = V _{SS} (Note 1)
Input Offset Drift with Temperature	$\Delta V_{OS} / \Delta T_A$	—	±2.0	—	µV/°C	T_A = -40°C to +125°C, V _{CM} = V _{SS}
Power Supply Rejection Ratio	PSRR	_	86	_	dB	V _{CM} = V _{SS}
Input Bias Current and Impedance	•	•				
Input Bias Current:	Ι _Β	_	±1.0	_	pА	
Industrial Temperature	Ι _Β	_	19	_	pА	T _A = +85°C
Extended Temperature	Ι _Β	_	1100	_	pА	T _A = +125°C
Input Offset Current	I _{OS}	_	±1.0	_	pА	
Common-Mode Input Impedance	Z _{CM}	_	10 ¹³ 6	_	Ω pF	
Differential Input Impedance	Z _{DIFF}	_	10 ¹³ 3		Ω pF	
Common-Mode	•	•				
Common-Mode Input Range	V _{CMR}	$V_{SS} - 0.3$	_	V _{DD} + 0.3	V	
Common-Mode Rejection Ratio	CMRR	60	76		dB	V_{CM} = -0.3V to 5.3V, V_{DD} = 5V
Open-Loop Gain	<u>.</u>					
DC Open-Loop Gain (Large Signal)	A _{OL}	88	112	—	dB	$V_{OUT} = 0.3V$ to $V_{DD} - 0.3V$, $V_{CM} = V_{SS}$
Output	<u>.</u>					
Maximum Output Voltage Swing	V _{OL} , V _{OH}	V _{SS} + 25	_	V _{DD} – 25	mV	V _{DD} = 5.5V, 0.5V input overdrive
Output Short-Circuit Current	I _{SC}	_	±6	_	mA	V _{DD} = 1.8V
	-	—	±23	—	mA	V _{DD} = 5.5V
Power Supply						•
Supply Voltage	V _{DD}	1.8	—	6.0	V	Note 2
Quiescent Current per Amplifier	Ι _Q	50	100	170	μA	I _O = 0, V _{DD} = 5.5V, V _{CM} = 5V

Note 1: MCP6001/1R/1U/2/4 parts with date codes prior to December 2004 (week code 49) were tested to ±7 mV minimum/maximum limits.

2: All parts with date codes November 2007 and later have been screened to ensure operation at V_{DD} = 6.0V. However, the other minimum and maximum specifications are measured at 1.8V and 5.5V.

AC ELECTRICAL SPECIFICATIONS

	Electrical Characteristics: Unless otherwise indicated, $T_A = +25^{\circ}$ C, $V_{DD} = +1.8$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_L = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L and $C_L = 60 \text{ pF}$ (refer to Figure 1-1).							
Parameters	Sym	Min	Тур	Max	Units	Conditions		
AC Response								
Gain Bandwidth Product	GBWP		1.0	_	MHz			
Phase Margin	PM	_	90	_	0	G = +1 V/V		
Slew Rate	SR	_	0.6		V/µs			
Noise						·		
Input Noise Voltage	E _{ni}		6.1	_	µVp-p	f = 0.1 Hz to 10 Hz		
Input Noise Voltage Density	e _{ni}		28		nV/√Hz	f = 1 kHz		
Input Noise Current Density	i _{ni}		0.6	—	fA/√Hz	f = 1 kHz		

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V and V_{SS} = GND.							
Parameters	Sym	Min	Тур	Max	Units	Conditions	
Temperature Ranges							
Industrial Temperature Range	T _A	-40	_	+85	°C		
Extended Temperature Range	Τ _Α	-40	—	+125	°C		
Operating Temperature Range	T _A	-40	—	+125	°C	Note 1	
Storage Temperature Range	T _A	-65		+150	°C		
Thermal Package Resistances							
Thermal Resistance, 5-Lead SC70	θ_{JA}		331		°C/W		
Thermal Resistance, 5-Lead SOT-23	θ_{JA}	_	256	_	°C/W		
Thermal Resistance, 8-Lead PDIP	θ_{JA}	_	85	_	°C/W		
Thermal Resistance, 8-Lead SOIC (150 mil)	θ_{JA}		163		°C/W		
Thermal Resistance, 8-Lead MSOP	θ_{JA}	_	206	_	°C/W		
Thermal Resistance, 8-Lead DFN (2x3)	θ_{JA}		68		°C/W		
Thermal Resistance, 14-Lead PDIP	θ_{JA}		70		°C/W		
Thermal Resistance, 14-Lead SOIC	θ_{JA}	_	120	_	°C/W		
Thermal Resistance, 14-Lead TSSOP	θ_{JA}	—	100	—	°C/W		

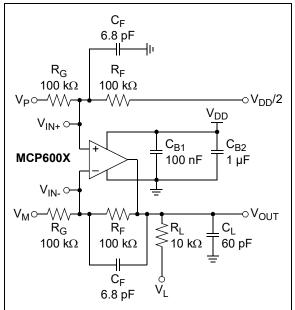
Note 1: The industrial temperature devices operate over this extended temperature range, but with reduced performance. In any case, the internal Junction Temperature (T_J) must not exceed the Absolute Maximum specification of +150°C.

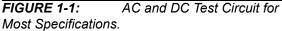
1.1 Test Circuits

The circuit used for most DC and AC tests is shown in Figure 1-1. This circuit can independently set V_{CM} and V_{OUT}; see Equation 1-1. Note that V_{CM} is not the circuit's Common-mode voltage ((V_P + V_M)/2) and that V_{OST} includes V_{OS} plus the effects (on the input offset error, V_{OST}) of temperature, CMRR, PSRR and A_{OL}.

EQUATION 1-1:

$$\begin{split} G_{DM} &= R_F / R_G \\ V_{CM} &= (V_P + V_{DD} / 2) / 2 \\ V_{OST} &= V_{IN-} - V_{IN+} \\ V_{OUT} &= (V_{DD} / 2) + (V_P - V_M) + V_{OST} (1 + G_{DM}) \\ \end{split}$$
Where: $G_{DM} &= \text{Differential-Mode Gain} \qquad (V/V) \\ V_{CM} &= \text{Op Amp's Common-Mode} \qquad (V) \\ \text{Input Voltage} \\ V_{OST} &= \text{Op Amp's Total Input Offset} \qquad (mV) \\ \text{Voltage} \end{split}$





NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $T_A = +25^{\circ}C$, $V_{DD} = +1.8V$ to +5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L and $C_L = 60 \text{ pF}$.

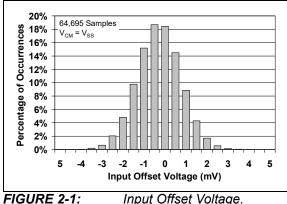


FIGURE 2-1:

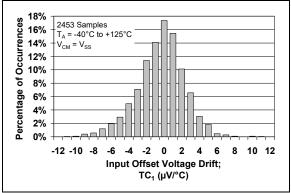
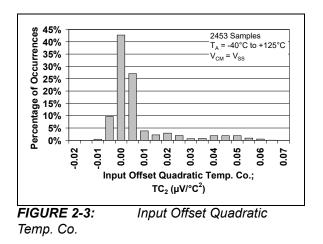
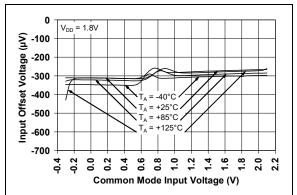


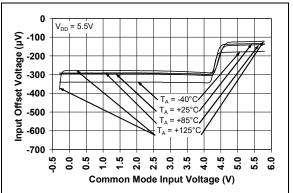
FIGURE 2-2:

Input Offset Voltage Drift.

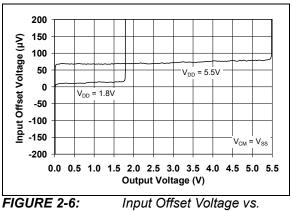




Input Offset Voltage vs. FIGURE 2-4: Common-Mode Input Voltage at V_{DD} = 1.8V.

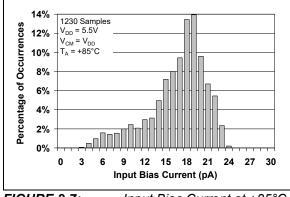


Input Offset Voltage vs. FIGURE 2-5: Common-Mode Input Voltage at V_{DD} = 5.5V.



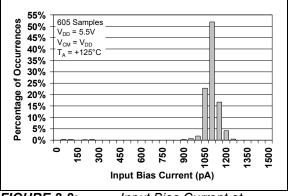
Output Voltage.

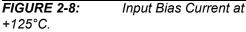
Note: Unless otherwise indicated, $T_A = +25^{\circ}C$, $V_{DD} = +1.8V$ to +5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L and $C_L = 60 \text{ pF}$.











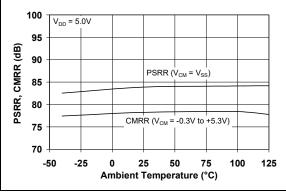


FIGURE 2-9: CMRR, PSRR vs. Ambient Temperature.

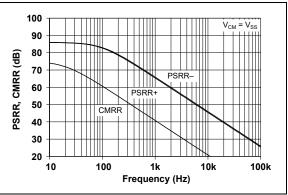


FIGURE 2-10: Frequency.

PSRR, CMRR vs.

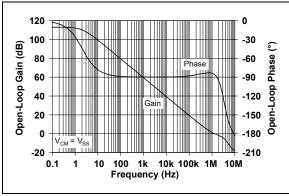


FIGURE 2-11: Open-Loop Gain, Phase vs. Frequency.

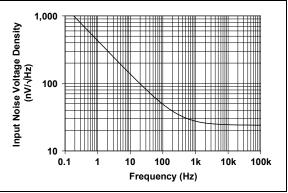


FIGURE 2-12: Input Noise Voltage Density vs. Frequency.

Note: Unless otherwise indicated, $T_A = +25^{\circ}C$, $V_{DD} = +1.8V$ to +5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L and $C_L = 60 \text{ pF}$.

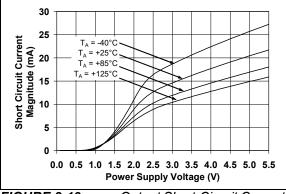


FIGURE 2-13: Output Short-Circuit Current vs. Power Supply Voltage.

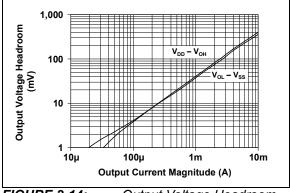


FIGURE 2-14: Output Voltage Headroom vs. Output Current Magnitude.

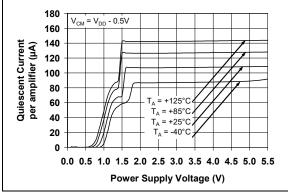


FIGURE 2-15: Quiescent Current vs. Power Supply Voltage.

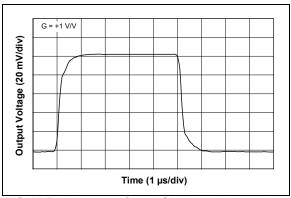


FIGURE 2-16: Small-Signal, Noninverting Pulse Response.

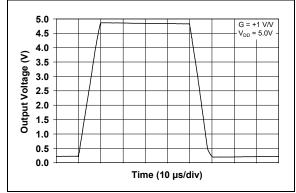


FIGURE 2-17: Large-Signal, Noninverting Pulse Response.

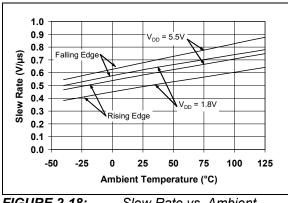


FIGURE 2-18: Temperature.

Slew Rate vs. Ambient

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = $V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L and $C_L = 60 \text{ pF}$.

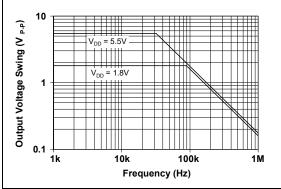
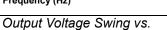


FIGURE 2-19: Frequency.



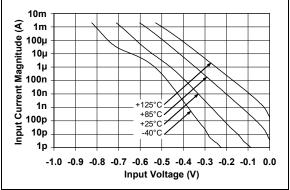


FIGURE 2-20: Measured Input Current vs. Input Voltage (below V_{SS}).

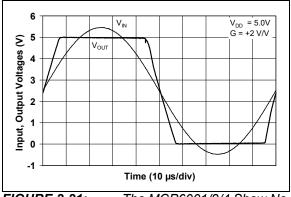


FIGURE 2-21: The MCP6001/2/4 Show No Phase Reversal.

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

MCP6001	MCP6001R	MCP6001U	MCP60	02	MCP6004		
5-Lead SC70, SOT-23	5-Lead SOT-23	5-Lead SOT-23	8-Lead MSOP, PDIP, SOIC	8-Lead 2x3 DFN		Symbol	Description
1	1	4	1	1	1	V _{OUT} , V _{OUTA}	Analog Output (Op Amp A)
4	4	3	2	2	2	V _{IN} -, V _{INA} -	Inverting Input (Op Amp A)
3	3	1	3	3	3	V _{IN} +, V _{INA} +	Noninverting Input (Op Amp A)
5	2	5	8	8	4	V _{DD}	Positive Power Supply
—	_		5	5	5	V _{INB} +	Noninverting Input (Op Amp B)
_	_	_	6	6	6	V _{INB} -	Inverting Input (Op Amp B)
_	_	_	7	7	7	V _{OUTB}	Analog Output (Op Amp B)
_	—	_	_	—	8	V _{OUTC}	Analog Output (Op Amp C)
_	_	_	_	—	9	V _{INC} -	Inverting Input (Op Amp C)
_	_	_	_	—	10	V _{INC} +	Noninverting Input (Op Amp C)
2	5	2	4	4	11	V _{SS}	Negative Power Supply
	_	_	_		12	V _{IND} +	Noninverting Input (Op Amp D)
	_		_	—	13	V _{IND} -	Inverting Input (Op Amp D)
—	—		_		14	V _{OUTD}	Analog Output (Op Amp D)
_	—	—	—	9	—	EP	Exposed Thermal Pad (EP); must be connected to V _{SS} .

TABLE 3-1: PIN FUNCTION TABLE

3.1 Analog Outputs

The output pins are low-impedance voltage sources.

3.2 Analog Inputs

The noninverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins

The positive power supply (V_{DD}) is 1.8V to 6.0V higher than the negative power supply (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

3.4 Exposed Thermal Pad (EP)

There is an internal electrical connection between the Exposed Thermal Pad (EP) and the V_{SS} pin; they must be connected to the same potential on the Printed Circuit Board (PCB).

NOTES:

4.0 APPLICATION INFORMATION

The MCP6001/2/4 family of op amps is manufactured using Microchip's state-of-the-art CMOS process and is specifically designed for low-cost, low-power and general purpose applications. The low supply voltage, low quiescent current and wide bandwidth makes the MCP6001/2/4 ideal for battery-powered applications. These devices have high phase margin, which makes them stable for larger capacitive load applications.

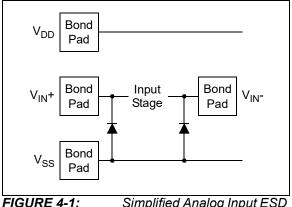
4.1 Rail-to-Rail Inputs

4.1.1 PHASE REVERSAL

The MCP6001/1R/1U/2/4 op amp is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-21 shows the input voltage exceeding the supply voltage without any phase reversal.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors and to minimize Input Bias (I_B) current. The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS} . They also clamp any voltages that go too far above V_{DD} ; their breakdown voltage is high enough to allow normal operation and low enough to bypass quick ESD events within the specified limits.



Structures.

Simplified Analog Input ESD

In order to prevent damage and/or improper operation of these op amps, the circuit they are in must limit the currents and voltages at the V_{IN}+ and V_{IN}- pins (see **Absolute Maximum Ratings†** at the beginning of **Section 1.0 "Electrical Characteristics**"). Figure 4-2 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins (V_{IN}+ and V_{IN}-) from going too far below ground, and the resistors, R₁ and R₂, limit the possible current drawn out of the input pins. Diodes, D₁ and D₂, prevent the input pins (V_{IN}+ and V_{IN}-) from going too far above

 $V_{DD},\,$ and dump any currents onto $V_{DD}.$ When implemented as shown, resistors, R_1 and R_2 , also limit the current through D_1 and $D_2.$

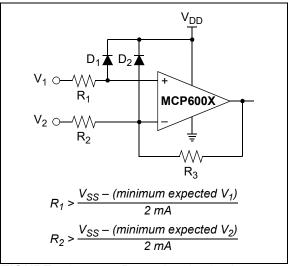


FIGURE 4-2: Protecting the Analog Inputs.

It is also possible to connect the diodes to the left of resistors, R₁ and R₂. In this case, current through the diodes, D₁ and D₂, needs to be limited by some other mechanism. The resistors then serve as inrush current limiters; the DC current into the input pins (V_{IN}+ and V_{IN}-) should be very small.

A significant amount of current can flow out of the inputs when the Common-Mode Voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-20. Applications that are high-impedance may need to limit the usable voltage range.

4.1.3 NORMAL OPERATION

The input stage of the MCP6001/1R/1U/2/4 op amps use two differential CMOS input stages in parallel. One operates at low Common-mode input voltage (V_{CM}), while the other operates at high V_{CM}. With this topology, the device operates with V_{CM} up to 0.3V above V_{DD} and 0.3V below V_{SS}.

The transition between the two input stages occurs when $V_{CM} = V_{DD} - 1.1V$. For the best distortion and gain linearity, with noninverting gains, avoid this region of operation.

4.2 Rail-to-Rail Output

The output voltage range of the MCP6001/2/4 op amps is V_{DD} - 25 mV (minimum), and V_{SS} + 25 mV (maximum) when R_L = 10 k Ω is connected to V_{DD}/2 and V_{DD} = 5.5V. Refer to Figure 2-14 for more information.

4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. While a unity gain buffer (G = +1) is the most sensitive to capacitive loads, all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., >100 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-3) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitance load.

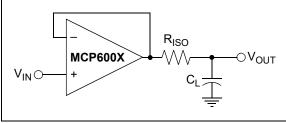


FIGURE 4-3: Output Resistor, R_{ISO}, Stabilizes Large Capacitive Loads.

Figure 4-4 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For noninverting gains, G_N and the signal gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

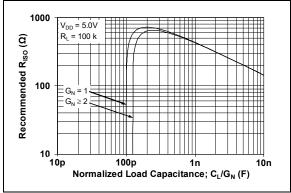


FIGURE 4-4: Recommended R_{ISO} Values for Capacitive Loads.

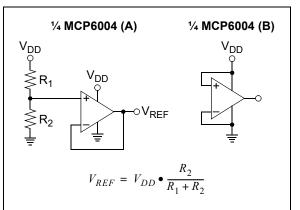
After selecting R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify R_{ISO} 's value until the response is reasonable. Bench evaluation and simulations with the MCP6001/1R/1U/2/4 SPICE macro model are very helpful.

4.4 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 μ F to 0.1 μ F) within 2 mm for good high-frequency performance. It also needs a bulk capacitor (i.e., 1 μ F or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with nearby analog parts.

4.5 Unused Op Amps

An unused op amp in a quad package (MCP6004) should be configured as shown in Figure 4-5. These circuits prevent the output from toggling and causing crosstalk. Circuit A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp; the op amp buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.





4.6 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow, which is greater than the MCP6001/1R/1U/2/4 family's bias current at +25°C (typically 1 pA).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-6.

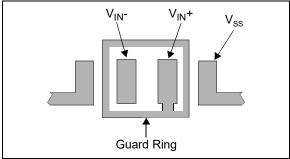


FIGURE 4-6: Example Guard Ring Layout for Inverting Gain.

- 1. Noninverting Gain and Unity Gain Buffer:
 - a. Connect the noninverting pin (V_{\rm IN}+) to the input with a wire that does not touch the PCB surface.
 - b. Connect the guard ring to the inverting input pin (V_{IN} -). This biases the guard ring to the Common-mode input voltage.
- 2. Inverting Gain and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors):
 - a. Connect the guard ring to the noninverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op amp (e.g., V_{DD}/2 or ground).
 - b. Connect the inverting pin (V $_{\rm IN}\text{-})$ to the input with a wire that does not touch the PCB surface.

4.7 Application Circuits

4.7.1 UNITY GAIN BUFFER

The rail-to-rail input and output capability of the MCP6001/2/4 op amp is ideal for unity gain buffer applications. The low quiescent current and wide bandwidth makes the device suitable for a buffer configuration in an instrumentation amplifier circuit, as shown in Figure 4-7.

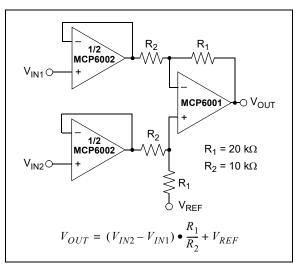


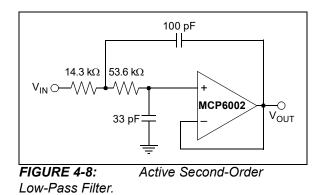
FIGURE 4-7: Instrumentation Amplifier with Unity Gain Buffer Inputs.

4.7.2 ACTIVE LOW-PASS FILTER

The MCP6001/2/4 op amp's low input bias current makes it possible for the designer to use larger resistors and smaller capacitors for active low-pass filter applications. However, as the resistance increases, the noise generated also increases. Parasitic capacitances and the large value resistors could also modify the frequency response. These trade-offs need to be considered when selecting circuit elements.

Usually, the op amp bandwidth is 100x the filter cutoff frequency (or higher) for good performance. It is possible to have the op amp bandwidth 10x higher than the cutoff frequency, thus having a design that is more sensitive to component tolerances.

Figure 4-8 shows a second-order Butterworth filter with 100 kHz cutoff frequency and a gain of +1 V/V; the op amp bandwidth is only 10x higher than the cutoff frequency. The component values were selected using Microchip's FilterLab[®] software.



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4.7.3 PEAK DETECTOR

The MCP6001/2/4 op amp has a high input impedance, rail-to-rail input/output and low input bias current, which makes this device suitable for peak detector applications. Figure 4-9 shows a peak detector circuit with clear and sample switches. The peak detection cycle uses a clock (CLK), as shown in Figure 4-9.

At the rising edge of the CLK, the sample switch closes to begin sampling. The peak voltage stored on C₁ is sampled to C₂ for a sample time defined by t_{SAMP}. At the end of the sample time (falling edge of sample signal), the clear signal goes high and closes the clear switch. When the clear switch closes, C₁ discharges through R₁ for a time defined by t_{CLEAR}. At the end of the clear time (falling edge of the clear signal), Op Amp A begins to store the peak value of V_{IN} on C₁ for a time defined by t_{DETECT}.

In order to define t_{SAMP} and t_{CLEAR} , it is necessary to determine the capacitor charging and discharging period. The capacitor charging time is limited by the amplifier source current, while the discharging time (τ) is defined using R_1 ($\tau = R_1C_1$). t_{DETECT} is the time that the input signal is sampled on C_1 and is dependent on the input voltage change frequency.

The op amp output current limit, and the size of the storage capacitors (both C_1 and C_2), could create slewing limitations as the Input Voltage (V_{IN}) increases. Current through a capacitor is dependent on the size of the capacitor and the rate of voltage change. From this relationship, the rate of voltage change or the slew rate

can be determined. For example, with an op amp short-circuit current of I_{SC} = 25 mA and a load capacitor of C_1 = 0.1 µF, then:

EQUATION 4-1:

$$I_{SC} = C_1 \frac{dV_{C1}}{dt}$$
$$\frac{dV_{C1}}{dt} = \frac{I_{SC}}{C_1}$$
$$= \frac{25mA}{0.1\mu F}$$
$$\frac{dV_{C1}}{dt} = 250mV/\mu s$$

This voltage rate of change is less than the MCP6001/2/4 slew rate of 0.6 V/ μ s. When the input voltage swings below the voltage across C₁, D₁ becomes reverse-biased. This opens the feedback loop and rails the amplifier. When the input voltage increases, the amplifier recovers at its slew rate. Based on the rate of voltage change shown in the above equation, it takes an extended period of time to charge a 0.1 μ F capacitor. The capacitors need to be selected so that the circuit is not limited by the amplifier slew rate. Therefore, the capacitors should be less than 40 μ F and a stabilizing resistor (R_{ISO}) needs to be properly selected. (Refer to Section 4.3 "Capacitive Loads".)

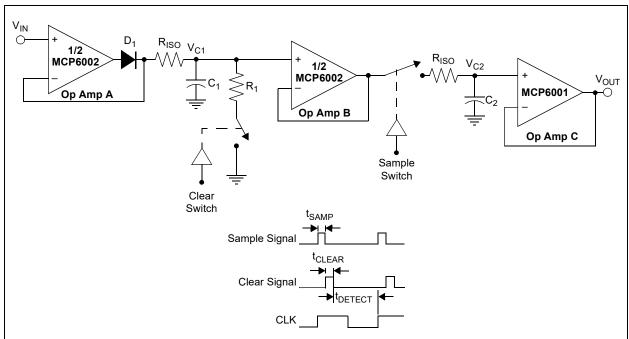


FIGURE 4-9: Peak Detector with Clear and Sample CMOS Analog Switches.

5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP6001/1R/1U/2/4 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6001/1R/1U/2/4 op amps is available on the Microchip website at www.microchip.com. The model was written and tested in official $OrCAD^{TM}$ (Cadence[®]) owned PSpice[®]. For the other simulators, it may require translation.

The model covers a wide aspect of the op amp's electrical specifications. Not only does the model cover voltage, current and resistance of the op amp, but it also covers the temperature and noise effects on the behavior of the op amp. The model has not been verified outside of the specification range listed in the op amp data sheet. The model behaviors under these conditions can not be ensured that it will match the actual op amp performance.

Moreover, the model is intended to be an initial design tool. Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab[®] Software

Microchip's FilterLab[®] software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip website at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 Mindi[™] Circuit Designer and Analog Simulator

Microchip's Mindi[™] Circuit Designer and Analog Simulator aids in the design of various circuits useful for active filter, amplifier and power management applications. It is a free online circuit designer and simulator available from the Microchip website at www.microchip.com/mindi. This interactive circuit designer and analog simulator enables designers to quickly generate circuit diagrams and simulate circuits. Circuits developed using the Mindi Circuit Designer and Analog Simulator can be downloaded to a personal computer or workstation.

5.4 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/ maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Data Sheets, Purchase and Sampling of Microchip parts.

5.5 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip website at www.microchip.com/analogtools.

Some boards that are especially useful are:

- MCP6XXX Amplifier Evaluation Board 1
- MCP6XXX Amplifier Evaluation Board 2
- MCP6XXX Amplifier Evaluation Board 3
- MCP6XXX Amplifier Evaluation Board 4
- · Active Filter Demo Board Kit
- 5/6-Pin SOT-23 Evaluation Board, P/N VSUPEV2
- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board, P/N SOIC8EV
- 14-Pin SOIC/TSSOP/DIP Evaluation Board, P/N SOIC14EV

5.6 Application Notes

The following Microchip Analog Design Note and Application Notes are available on the Microchip website at www.microchip.com/appnotes and are recommended as supplemental reference resources.

- ADN003: "Select the Right Operational Amplifier for your Filtering Circuits" (DS21821)
- AN722: "Operational Amplifier Topologies and DC Specifications" (DS00722)
- AN723: "Operational Amplifier AC Specifications and Applications" (DS00723)
- AN884: "Driving Capacitive Loads With Op Amps" (DS00884)

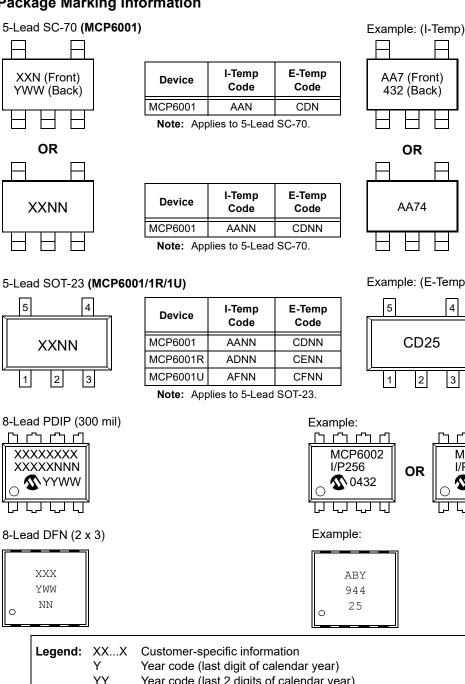
- AN990: "Analog Sensor Conditioning Circuits An Overview" (DS00990)
- AN1177: "Op Amp Precision Design: DC Errors" (DS01177)
- AN1228: "Op Amp Precision Design: Random Noise" (DS01228)
- AN1297: "Microchip's Op Amp SPICE Macro Models" (DS01297)

These application notes and others are listed in the design guide:

• "Signal Chain Design Guide" (DS21825)

6.0 PACKAGING INFORMATION

6.1 **Package Marking Information**



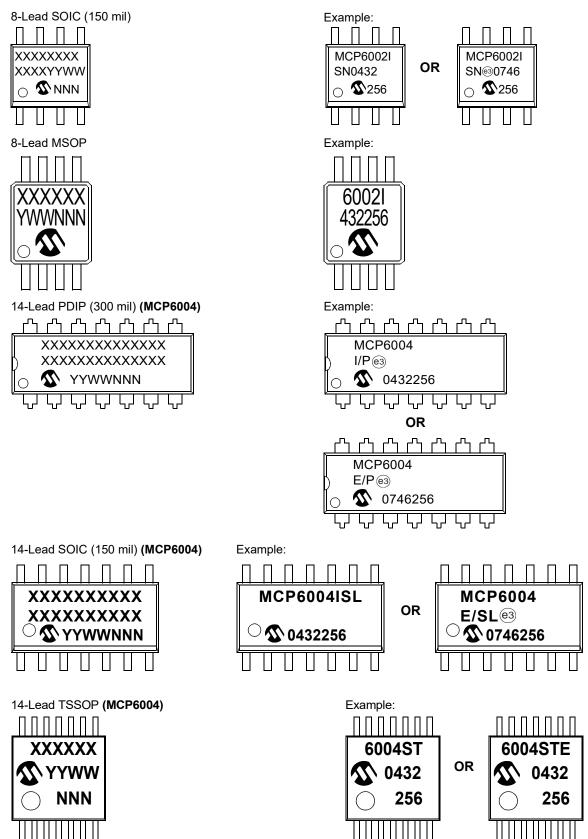
Example: (E-Temp)

5	;		4	
	С	D25		
1		2	3	

MCP6002 I/P@256 **1**0746

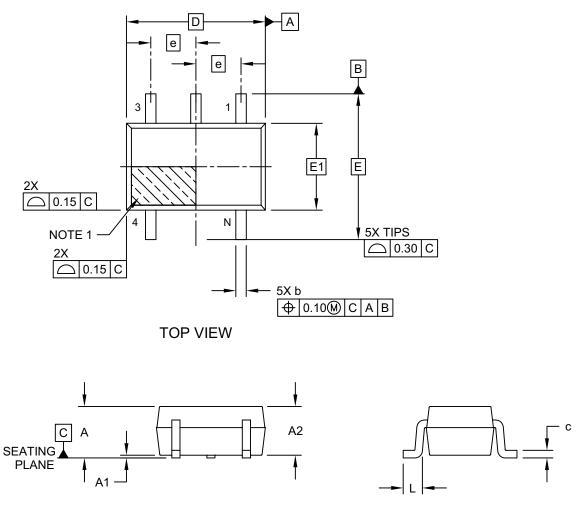
Legend	: XXX Y YY WW NNN @3 *	Customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	be carrie	nt the full Microchip part number cannot be marked on one line, it will d over to the next line, thus limiting the number of available s for customer-specific information.

Package Marking Information (Continued)



5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



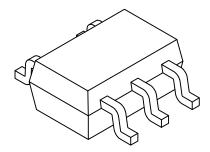
SIDE VIEW

END VIEW

Microchip Technology Drawing C04-061-LT Rev E Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Number of Pins	Ν		5	
Pitch	е		0.65 BSC	
Overall Height	Α	0.80	-	1.10
Standoff	A1	0.00	-	0.10
Molded Package Thickness	A2	0.80	-	1.00
Overall Length	D		2.00 BSC	
Overall Width	Е		2.10 BSC	
Molded Package Width	E1		1.25 BSC	
Terminal Width	b	0.15	-	0.40
Terminal Length	L	0.10	0.20	0.46
Lead Thickness	С	0.08	-	0.26

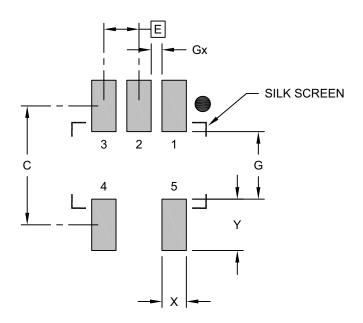
Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- 3. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-061-LT Rev E Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	Ν	ILLIMETER	S
Dimension	Dimension Limits		NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	С		2.20	
Contact Pad Width	Х			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

Notes:

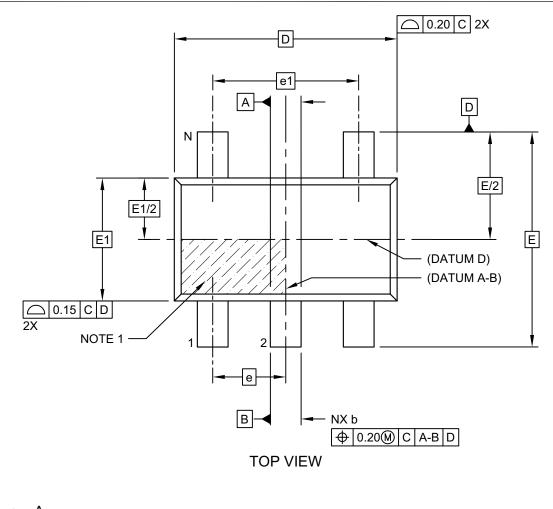
1. Dimensioning and tolerancing per ASME Y14.5M

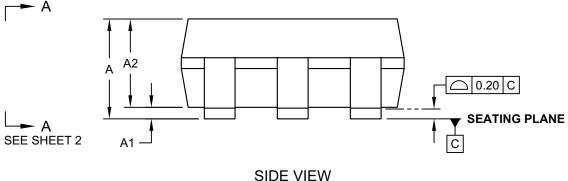
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061-LT Rev E

5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

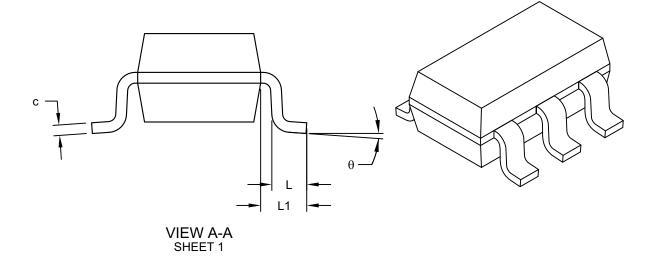




Microchip Technology Drawing C04-091-OT Rev F Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS			
Dimension I	_imits	MIN	NOM	MAX	
Number of Pins	Ν		5		
Pitch	е		0.95 BSC		
Outside lead pitch	e1		1.90 BSC		
Overall Height	Α	0.90	-	1.45	
Molded Package Thickness	A2	0.89	-	1.30	
Standoff	A1	-	-	0.15	
Overall Width	E	2.80 BSC			
Molded Package Width	E1		1.60 BSC		
Overall Length	D		2.90 BSC		
Foot Length	L	0.30	-	0.60	
Footprint	L1	0.60 REF			
Foot Angle	ø	0°	-	10°	
Lead Thickness	С	0.08	-	0.26	
Lead Width	b	0.20	-	0.51	

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.

2. Dimensioning and tolerancing per ASME Y14.5M

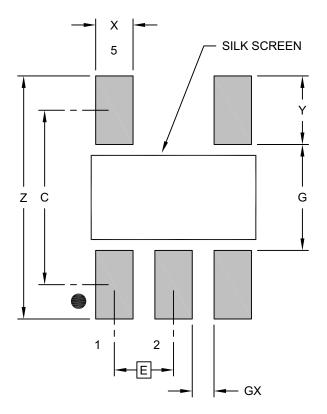
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-OT Rev F Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units			S	
Dimension	Limits	MIN	NOM	MAX	
Contact Pitch	E		0.95 BSC		
Contact Pad Spacing	С		2.80		
Contact Pad Width (X5)	Х			0.60	
Contact Pad Length (X5) Y				1.10	
Distance Between Pads	G	1.70			
Distance Between Pads	GX	0.35			
Overall Width	Z			3.90	

Notes:

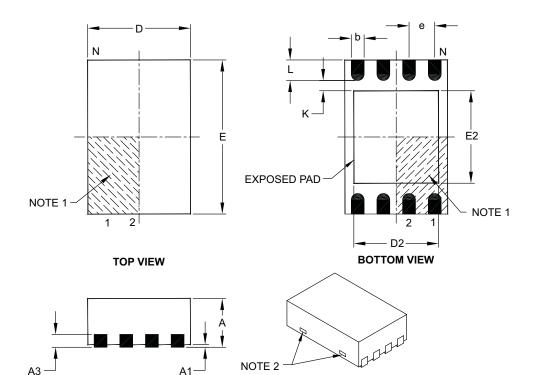
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091-OT Rev F

8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX	
Number of Pins	N		8		
Pitch	е		0.50 BSC		
Overall Height	А	0.80	0.90	1.00	
Standoff	A1	0.00	0.02	0.05	
Contact Thickness	A3	0.20 REF			
Overall Length	D	2.00 BSC			
Overall Width	E	3.00 BSC			
Exposed Pad Length	D2	1.30	-	1.55	
Exposed Pad Width	E2	1.50	_	1.75	
Contact Width	b	0.20	0.25	0.30	
Contact Length	L	0.30	0.40	0.50	
Contact-to-Exposed Pad	К	0.20	_	_	

Notes:

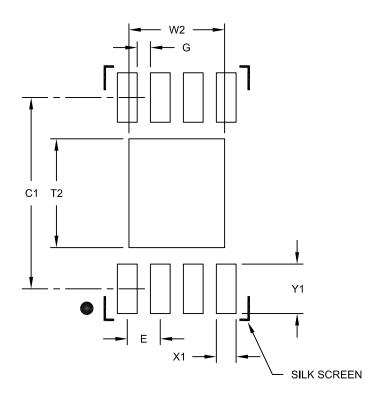
- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package may have one or more exposed tie bars at ends.
- 3. Package is saw singulated.
- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123C

8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS			
Dimension Limits		MIN	NOM	MAX	
Contact Pitch	E	0.50 BSC			
Optional Center Pad Width	W2			1.45	
Optional Center Pad Length	T2			1.75	
Contact Pad Spacing	C1	2.90			
Contact Pad Width (X8)	X1			0.30	
Contact Pad Length (X8)	Y1			0.75	
Distance Between Pads	G	0.20			

Notes:

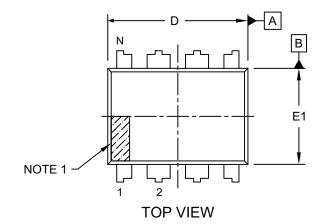
1. Dimensioning and tolerancing per ASME Y14.5M

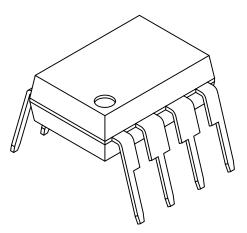
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

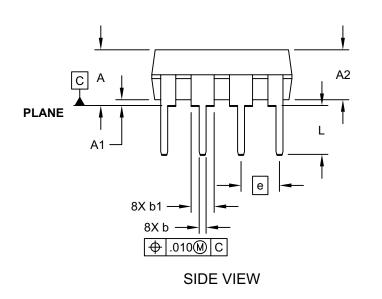
Microchip Technology Drawing No. C04-2123B

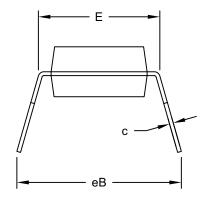
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging







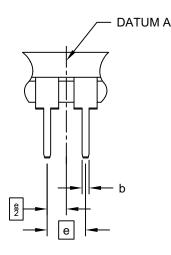


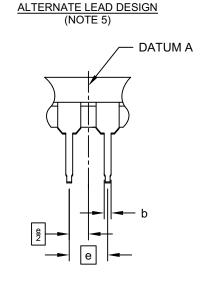
END VIEW

Microchip Technology Drawing No. C04-018-P Rev E Sheet 1 of 2

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





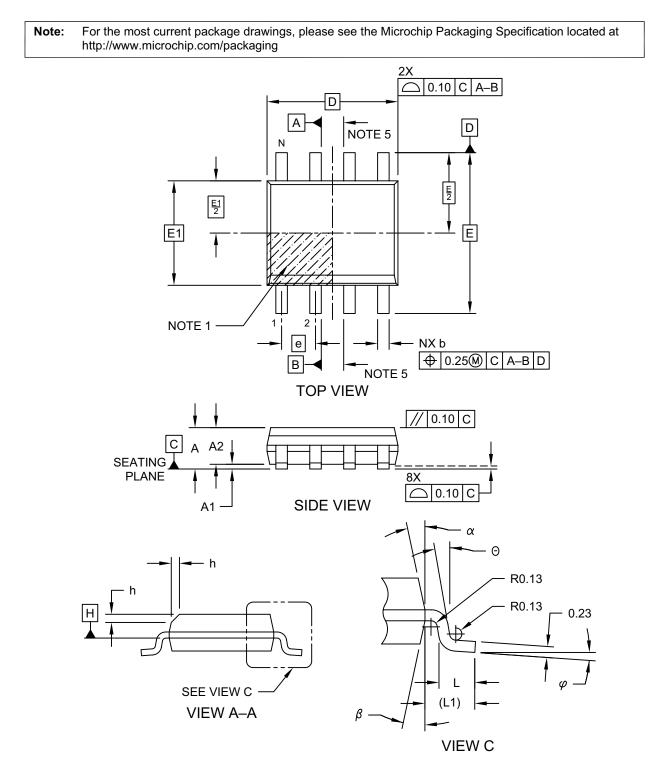
Units		INCHES			
Dimension Limits		MIN	NOM	MAX	
Number of Pins	N	8			
Pitch	е	.100 BSC			
Top to Seating Plane	Α	-	-	.210	
Molded Package Thickness	A2	.115	.130	.195	
Base to Seating Plane	A1	.015	-	-	
Shoulder to Shoulder Width	Е	.290	.310	.325	
Molded Package Width	E1	.240	.250	.280	
Overall Length	D	.348	.365	.400	
Tip to Seating Plane	L	.115	.130	.150	
Lead Thickness	С	.008	.010	.015	
Upper Lead Width	b1	.040	.060	.070	
Lower Lead Width	b	.014	.018	.022	
Overall Row Spacing §	eВ	-	-	.430	

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M
- BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- 5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-P Rev E Sheet 2 of 2

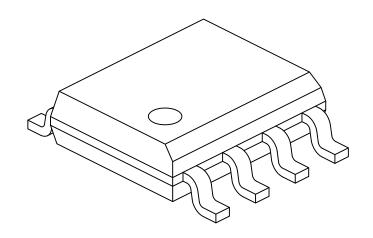
8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]



Microchip Technology Drawing No. C04-057-SN Rev E Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS			
Dimension Limits		MIN	NOM	MAX	
Number of Pins	Ν	8			
Pitch	е	1.27 BSC			
Overall Height	А	-	-	1.75	
Molded Package Thickness	A2	1.25	-	-	
Standoff §	A1	0.10	-	0.25	
Overall Width	E	6.00 BSC			
Molded Package Width	E1	3.90 BSC			
Overall Length	D	4.90 BSC			
Chamfer (Optional)	h	0.25	-	0.50	
Foot Length	L	0.40	-	1.27	
Footprint	L1	1.04 REF			
Foot Angle	φ	0°	-	8°	
Lead Thickness	С	0.17	-	0.25	
Lead Width	b	0.31	-	0.51	
Mold Draft Angle Top	α	5°	-	15°	
Mold Draft Angle Bottom	β	5°	-	15°	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic

- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M BSC: Basic Dimension. Theoretically exact value shown without tolerances. BEE: Reference Dimension, usually without tolerance, for information purpose.

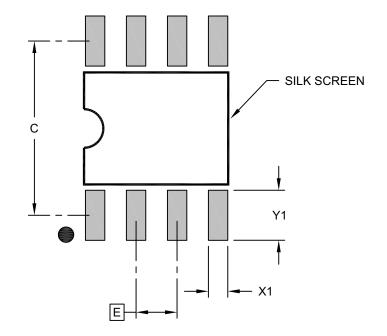
REF: Reference Dimension, usually without tolerance, for information purposes only.

5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev E Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	
Contact Pitch	E	1.27 BSC			
Contact Pad Spacing	С		5.40		
Contact Pad Width (X8)	X1			0.60	
Contact Pad Length (X8)	Y1			1.55	

Notes:

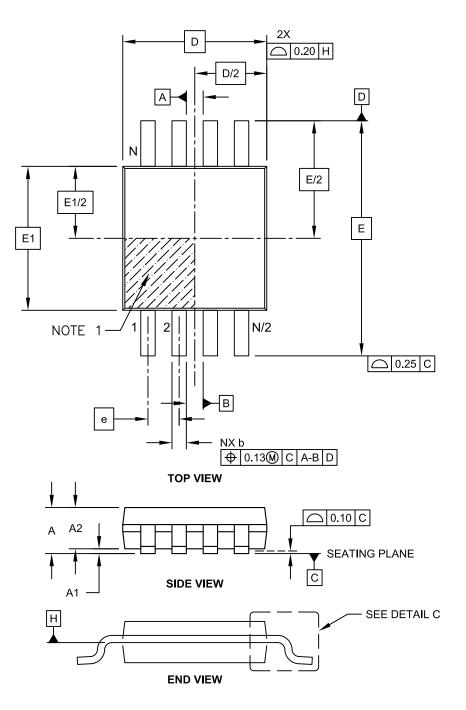
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev E

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

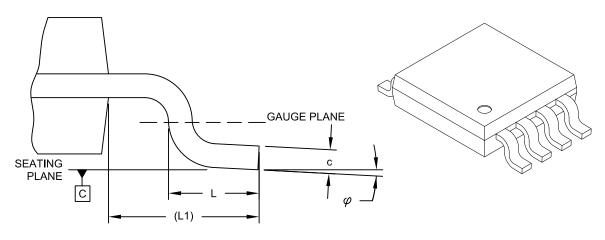
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-111C Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C

	MILLIMETERS			
Dimension Limits		MIN	NOM	MAX
Number of Pins	Ν		8	
Pitch	е	0.65 BSC		
Overall Height	Α	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Overall Length	D	3.00 BSC		
Foot Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	С	0.08	-	0.23
Lead Width	b	0.22	-	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side. 3. Dimensioning and tolerancing per ASME Y14.5M.

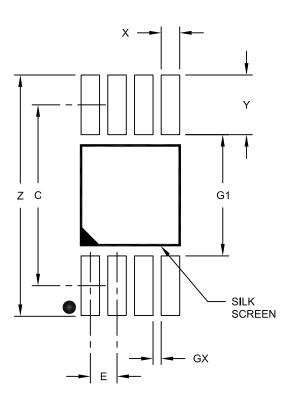
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units		MILLIMETERS			
Dimensio	Dimension Limits		NOM	MAX		
Contact Pitch	E	0.65 BSC				
Contact Pad Spacing	С		4.40			
Overall Width	Z			5.85		
Contact Pad Width (X8)	X1			0.45		
Contact Pad Length (X8)	Y1			1.45		
Distance Between Pads	G1	2.95				
Distance Between Pads	GX	0.20				

Notes:

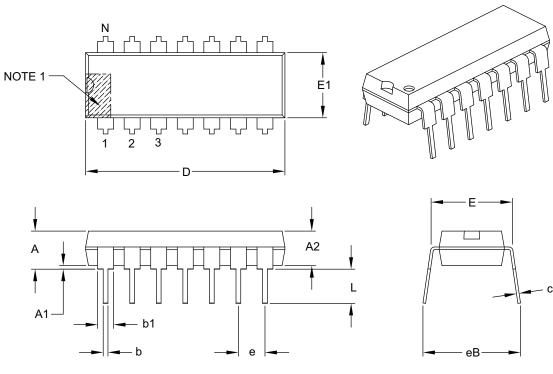
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	Ν	14		
Pitch	е	.100 BSC		
Top to Seating Plane	Α	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	с	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	_	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.

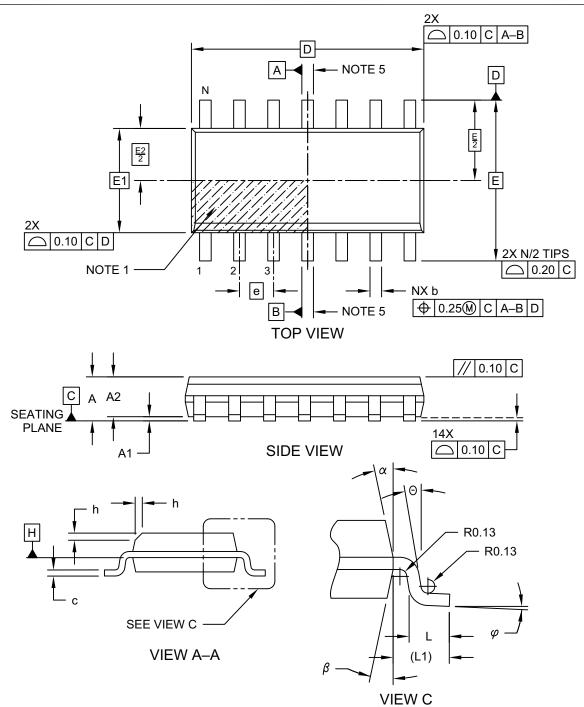
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

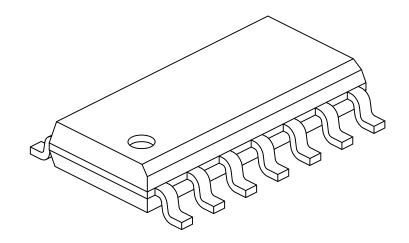
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-065-SL Rev D Sheet 1 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	Ν	14		
Pitch	е		1.27 BSC	
Overall Height	Α	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L 0.40 - 1.2		1.27	
Footprint	L1	1.04 REF		
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	С	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic

- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M BSC: Basic Dimension. Theoretically exact value shown without tolerances.

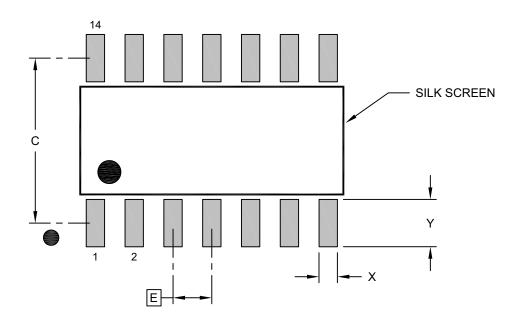
REF: Reference Dimension, usually without tolerance, for information purposes only.

5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065-SL Rev D Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		Ν	IILLIMETER	S
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	С		5.40	
Contact Pad Width (X14)	Х			0.60
Contact Pad Length (X14)	Y			1.55

Notes:

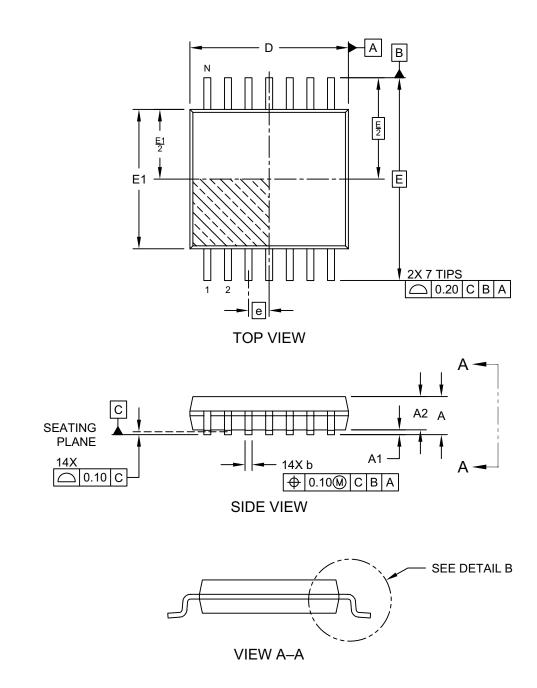
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065-SL Rev D

14Lead Thin Shrink Small Outline Package [ST] 4.4 mm Body [TSSOP]

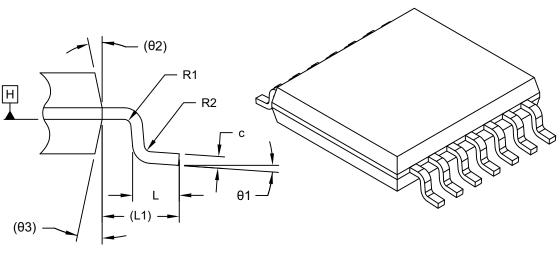
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-087 Rev D Sheet 1 of 2

14Lead Thin Shrink Small Outline Package [ST] 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	14		
Pitch	е	0.65 BSC		
Overall Height	Α	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.80	1.00	1.05
Overall Length	D	4.90	5.00	5.10
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Terminal Width	b	0.19	-	0.30
Terminal Thickness	С	0.09	-	0.20
Terminal Length	L	0.45	0.60	0.75
Footprint L1		1.00 REF		
Lead Bend Radius	R1	0.09	-	_
Lead Bend Radius	R2	0.09	-	-
Foot Angle	θ1	0°	_	8°
Mold Draft Angle	θ2	_	12° REF	_
Mold Draft Angle	θ3	_	12° REF	_

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Dimensioning and tolerancing per ASME Y14.5M

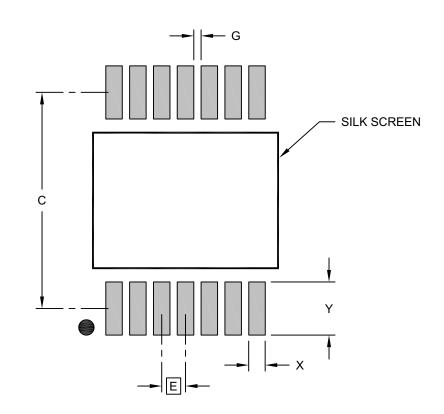
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087 Rev D Sheet 2 of 2

14Lead Thin Shrink Small Outline Package [ST] 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	E 0.65 BSC		
Contact Pad Spacing	С		5.90	
Contact Pad Width (Xnn)	Х			0.45
Contact Pad Length (Xnn)	Y			1.45
Contact Pad to Contact Pad (Xnn)	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2087 Rev D

MCP6001/1R/1U/2/4

NOTES:

APPENDIX A: REVISION HISTORY

Revision L (March 2020)

The following is the list of modifications:

 Updated package drawings for the 5-Lead SC-70 and 14-Lead TSSOP packages in Section 6.0 "Packaging Information".

Revision K (November 2019)

The following is the list of modifications:

1. Updated Section 6.0 "Packaging Information".

Revision J (November 2009)

The following is the list of modifications:

- 1. Added new 2x3 DFN 8-Lead package on page 1.
- 2. Updated the Temperature Specifications table with 2x3 DFN thermal resistance information.
- 3. Updated Section 1.1 "Test Circuits".
- 4. Updated Figure 2-15.
- 5. Added the 2x3 DFN column to Table 3-1.
- 6. Added new Section 3.4 "Exposed Thermal Pad (EP)".
- 7. Updated Section 5.1 "SPICE Macro Model".
- 8. Updated Section 5.5 "Analog Demonstration and Evaluation Boards".
- 9. Updated Section 5.6 "Application Notes".
- 10. Updated Section 6.1 "Package Marking Information" with the new 2x3 DFN package marking information.
- 11. Updated the package drawings.
- 12. Updated the Product Identification System section with new 2x3 DFN package information.

Revision H (May 2008)

The following is the list of modifications:

- 1. Section 5.0 "Design Aids": Name change for Mindi™ Simulation Tool.
- 2. Package Types: Correct device labeling error.
- 3. Section 1.0 "Electrical Characteristics", DC Electrical Specifications: Changed "Maximum Output Voltage Swing" condition from 0.9V Input Overdrive to 0.5V Input Overdrive.
- Section 1.0 "Electrical Characteristics", AC Electrical Specifications: Changed Phase Margin condition from G = +1 to G= +1 V/V.
- Section 5.0 "Design Aids": Name change for Mindi Simulation Tool.

Revision G (November 2007)

The following is the list of modifications:

- 1. Updated notes to **Section 1.0 "Electrical Characteristics"**.
- 2. Increased Absolute Maximum Voltage range at input pins.
- 3. Increased maximum operating supply voltage (V_{DD}) .
- 4. Added test circuits.
- 5. Added Figure 2-3 and Figure 2-20.
- 6. Added Section 4.1.1 "Phase Reversal", Section 4.1.2 "Input Voltage and Current Limits", Section 4.1.3 "Normal Operation" and Section 4.5 "Unused Op Amps".
- 7. Updated Section 5.0 "Design Aids",
- 8. Updated Section 6.0 "Packaging Information".
- 9. Updated Package Outline Drawings.

Revision F (March 2005)

The following is the list of modifications:

1. Updated Section 6.0 "Packaging Information" to include old and new packaging examples.

Revision E (December 2004)

The following is the list of modifications:

- V_{OS} specification reduced to ±4.5 mV from ±7.0 mV for parts starting with date code YYWW = 0449
- 2. Corrected package markings in Section 6.0 "Packaging Information".
- 3. Added Appendix A: Revision History.

Revision D (May 2003)

• Undocumented changes.

Revision C (December 2002)

• Undocumented changes.

Revision B (October 2002)

• Undocumented changes.

Revision A (June 2002)

Original data sheet release.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. X /XX		Examples:			
Device Temp	erature Package nge	a) MCP6001T-I/LT: Tape and Reel, Industrial Temperature, 5-Lead SC-70 Package.			
Device:	MCP6001T: Single Op Amp (Tape and Reel)	b) MCP6001T-I/OT: Tape and Reel, Industrial Temperature, 5-Lead SOT-23 Package.			
	(SC-70, SOT-23) MCP6001RT: Single Op Amp (Tape and Reel) (SOT-23) MCP6001UT: Single Op Amp (Tape and Reel) (SOT-23) MCP6002: Dual Op Amp	c) MCP6001RT-I/OT: Tape and Reel, Industrial Temperature, 5-Lead SOT-23 Package.			
	MCP6002T: Dual Op Amp (Tape and Reel) (SOIC, MSOP) MCP6004: Quad Op Amp	d) MCP6001UT-E/OT: Tape and Reel, Extended Temperature, 5-Lead SOT-23 Package.			
	MCP6004T: Quad Op Amp (Tape and Reel) (SOIC, MSOP)	a) MCP6002-I/MS: Industrial Temperature, 8-Lead MSOP Package.			
Temperature Range:	I = -40°C to +85°C E = -40°C to +125°C	b) MCP6002-I/P: Industrial Temperature, 8-Lead PDIP Package.			
		c) MCP6002-E/P: Extended Temperature, 8-Lead PDIP Package.			
Package:	LT = Plastic Small Outline Transistor (SC-70), 5-Lead (MCP6001 only)	d) MCP6002-E/MC: Extended Temperature, 8-Lead DFN Package.			
	OT = Plastic Small Outline Transistor (SOT-23), 5-Lead (MCP6001, MCP6001R, MCP6001U) MS = Plastic MSOP, 8-Lead	e) MCP6002-I/SN: Industrial Temperature, 8-Lead SOIC Package.			
	MC = Plastic Dual Flat, 2x3x0.9 mm (DFN), 8-Lead P = Plastic DIP, 300 mil Body (PDIP), 8-Lead, 14-Lead SN = Plastic SOIC (3.90 mm body), 8-Lead	f) MCP6002T-I/MS: Tape and Reel, Industrial Temperature, 8-Lead MSOP Package.			
	SL = Plastic SOIC (3.90 body), 14-Lead ST = Plastic TSSOP (4.4 mm body), 14-Lead	g) MCP6002T-E/MC: Tape and Reel, Extended Temperature, 8-Lead DFN Package.			
		a) MCP6004-I/P: Industrial Temperature, 14-Lead PDIP Package.			
		b) MCP6004-I/SL: Industrial Temperature, 14-Lead SOIC Package.			
		c) MCP6004-E/SL: Extended Temperature, 14-Lead SOIC Package.			
		d) MCP6004-I/ST: Industrial Temperature, 14-Lead TSSOP Package.			
		e) MCP6004T-I/SL: Tape and Reel, Industrial Temperature, 14-Lead SOIC Package.			
		f) MCP6004T-I/ST: Tape and Reel, Industrial Temperature, 14-Lead TSSOP Package.			

MCP6001/1R/1U/2/4

NOTES:

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