ISL95808

High Voltage Synchronous Rectified Buck MOSFET Driver

FN8689
Rev 2.00
May 25, 2016

The ISL95808 is a high frequency, dual MOSFET driver with low shutdown current, optimized to drive two N-Channel power MOSFETs in a synchronous-rectified buck converter topology. It is especially suited for mobile computing applications that require high efficiency and excellent thermal performance. The driver, combined with an Intersil multiphase Buck PWM controller, forms a complete single-stage core-voltage regulator solution for advanced mobile microprocessors.

The ISL95808 features a 4A typical sinking current for the lower gate driver. This current is capable of holding the lower MOSFET gate off during the rising edge of the phase node. This prevents shoot-through power loss caused by the high dv/dt of phase voltages. The operating voltage matches the 30V breakdown voltage of the MOSFETs commonly used in mobile computer power supplies.

The ISL95808 also features a three-state PWM input. This PWM input, working together with Intersil's multiphase PWM controllers, will prevent negative voltage output during CPU shutdown. This feature eliminates a protective Schottky diode usually seen in microprocessor power systems.

MOSFET gates can be efficiently switched up to 2MHz using the ISL95808. Each driver is capable of driving a 3000pF load with propagation delays of 8ns and transition times under 10ns. Bootstrapping is implemented with an internal Schottky diode. This reduces system cost and complexity, while allowing for the use of higher performance MOSFETs. Adaptive shoot–through protection is integrated to prevent both MOSFETs from conducting simultaneously.

A diode emulation feature is integrated in the ISL95808 to enhance converter efficiency at light load conditions. This feature also allows for monotonic start-up into prebiased outputs. When diode emulation is enabled, the driver will allow discontinuous conduction mode by detecting when the inductor current reaches zero and subsequently turning off the low-side MOSFET gate.

The ISL95808 also features very low shutdown supply current (5V, 3µA) to ensure the low power consumption.

Features

- Dual MOSFET drivers for synchronous rectified bridge
- Adaptive shoot-through protection
- 0.5Ω ON-resistance and 4A sink current capability
- Supports high switching frequency up to 2MHz
  - Fast output rise and fall time
  - Low propagation delay
- Three-state PWM input for power stage shutdown
- Internal bootstrap Schottky diode
- Low shutdown supply current (5V, 3µA)
- Diode emulation for enhanced light-load efficiency and prebiased start-up applications
- VCC POR (Power-On Reset) feature integrated
- Low three-state shutdown hold-off time (typical 160ns)
- DFN package
- Pb-free (RoHS compliant)

Applications

- Core voltage supplies for Intel® and AMD™ mobile microprocessors
- High frequency low profile DC/DC converters
- High current low output voltage DC/DC converters
- High input voltage DC/DC converters

Related Literature

- TB389, "PCB Land Pattern Design and Surface Mount Guidelines for MLFP Packages"
- TB447, "Guidelines for Preventing Boot-to-Phase Stress on Half-Bridge MOSFET Driver ICs"

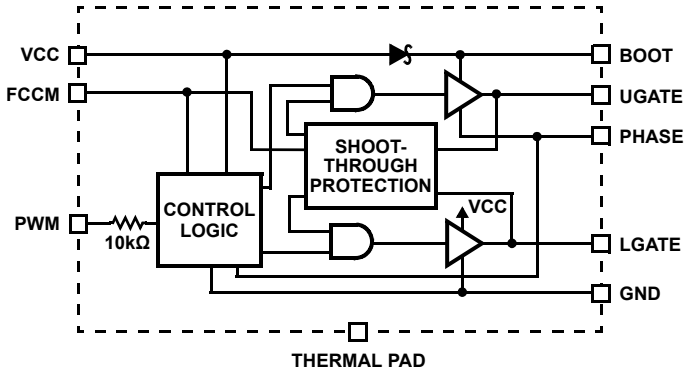


FIGURE 1. BLOCK DIAGRAM

Ordering Information

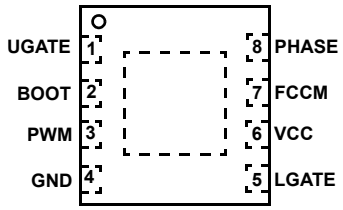
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (UNITS)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL95808HRZ-T	08	-10 to +100	6k	8 Ld 2x2 DFN	L8.2x2D
ISL95808IRZ-T	08I	-40 to +100	6k	8 Ld 2x2 DFN	L8.2x2D

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for ISL95808. For more information on MSL, please see tech brief TB363.

Pin Configuration

ISL95808
(8 LD 2x2 DFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	UGATE	The UGATE pin is the upper gate drive output. Connect to the gate of high-side power N-Channel MOSFET.
2	BOOT	BOOT is the floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See "Internal Bootstrap Diode" on page 7 for guidance in choosing the appropriate capacitor value.
3	PWM	The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation. See "Three-State PWM Input" on page 6 for further details. Connect this pin to the PWM output of the controller.
4	GND	GND is the ground pin for the IC.
5	LGATE	LGATE is the lower gate drive output. Connect to gate of the low-side power N-Channel MOSFET.
6	VCC	Connect the VCC pin to a +5V bias supply. Place a high quality bypass capacitor from this pin to GND. The VCC pin of the driver(s) and related VCC or +5V bias supply pin of the Intersil controller must share a common +5V supply.
7	FCCM	The FCCM pin enables or disables diode emulation. When FCCM is LOW, diode emulation is allowed. When FCCM is HIGH, continuous conduction mode is forced. See "Diode Emulation" on page 6 for more detail. High impedance on the input of FCCM will shut down ISL95808.
8	PHASE	Connect the PHASE pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin provides a return path for the upper gate driver.

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.3V to 7V
Input Voltage (V_{FCCM}, V_{PWM}) . . . . . -0.3V to VCC + 0.3V
BOOT Voltage ($V_{BOOT-GND}$) . . . . . -0.3V to 33V or 36V (<20ns)
BOOT To PHASE Voltage ($V_{BOOT-PHASE}$) . . . . . -0.3V to 7V (DC)
-0.3V to 9V (<10ns)
PHASE Voltage (Note 4) . . . . . (GND - 0.3V) to 30V
GND - 8V (<20ns Pulse Width, 10µJ)
UGATE Voltage . . . . . V_{PHASE} - 0.3V (DC) to V_{BOOT}
V_{PHASE} - 5V (<20ns Pulse Width, 10µJ) to V_{BOOT}
LGATE Voltage . . . . . GND - 0.3V (DC) to VCC + 0.3V
GND - 2.5V (<20ns Pulse Width, 5µJ) to VCC + 0.3V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld 2x2 DFN Package (Notes 5, 6)	87	22

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Temperature
HRZ . . . . . -10°C to +100°C
IRZ . . . . . -40°C to +100°C
Maximum Operating Junction Temperature . . . . . +125°C
Supply Voltage, VCC . . . . . 5V ±10%

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. The Phase Voltage is capable of withstanding -7V when the BOOT pin is at GND.
5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
6. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. **Boldface limits apply across the operating temperature range T_A = -40°C to +100°C for Industrial (IRZ) and T_A = -10°C to +100°C for HI-Temp Commercial (HRZ).**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
V_{CC} SUPPLY CURRENT						
I_{VCCSD}	Shutdown Bias Supply Current	PWM and FCCM pin floating	-	3.3	**4**	µA
I_{VCC}	Operating Bias Supply Current	PWM pin floating, V_{FCCM} = 5V	-	80	-	µA
		PWM pin floating, V_{FCCM} = 0V	-	120	-	µA
POR						
	V_{CC} Rising		-	3.40	**3.90**	V
HRZ	V_{CC} Falling		**2.40**	2.90	-	V
IRZ			**2.39**	2.90	-	V
	Hysteresis		-	500	-	mV
BOOTSTRAP DIODE						
HRZ	Forward Voltage	V_{VCC} = 5V, forward bias current = 2mA	**0.43**	0.55	**0.65**	V
IRZ		V_{VCC} = 5V, forward bias current = 2mA	**0.43**	0.55	**0.70**	V
PWM INPUT						
I_{PWM}	Input Current	V_{PWM} = 5V	-	250	-	µA
		V_{PWM} = 0V	-	-250	-	µA
	PWM Three-State Rising Threshold	V_{VCC} = 5V	**0.70**	1.00	**1.30**	V
	PWM Three-State Falling Threshold	V_{VCC} = 5V	**3.5**	3.8	**4.1**	V
HRZ	Three-State Shutdown Hold-Off Time	V_{VCC} = 5V, temperature = +25°C	100	175	250	ns
IRZ		V_{VCC} = 5V, temperature = +25°C	85	175	250	ns
FCCM INPUT						
I_{FCCM}	Input Current	V_{FCCM} = 5V	**-**	50	**-**	µA
		V_{FCCM} = 0V	**-**	50	**-**	µA
	FCCM Shutdown Rising Threshold	V_{VCC} = 5V	**1.4**	1.8	**2.2**	V

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. **Boldface limits apply across the operating temperature range T_A = -40°C to +100°C for Industrial (IRZ) and T_A = -10°C to +100°C for Hi-Temp Commercial (HRZ). (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
	FCCM Shutdown Falling Threshold	V_{VCC} = 5V	**2.8**	3.2	**3.6**	V
$t_{PS4EXIT}$	PS4 Exit Latency	V_{VCC} = 5V	-		**15**	µs
SWITCHING TIME						
t_{RU}	UGATE Rise Time (Note 7)	V_{VCC} = 5V, 3nF load	-	8.0	-	ns
t_{RL}	LGATE Rise Time (Note 7)	V_{VCC} = 5V, 3nF load	-	8.0	-	ns
t_{FU}	UGATE Fall Time (Note 7)	V_{VCC} = 5V, 3nF load	-	8.0	-	ns
t_{FL}	LGATE Fall Time (Note 7)	V_{VCC} = 5V, 3nF load	-	4.0	-	ns
t_{PDLU}	UGATE Turn-Off Propagation Delay	V_{VCC} = 5V, outputs unloaded	-	18	-	ns
t_{PDLL}	LGATE Turn-Off Propagation Delay	V_{VCC} = 5V, outputs unloaded	-	25	-	ns
t_{PDHU}	UGATE Turn-On Propagation Delay	V_{VCC} = 5V, outputs unloaded	**-**	20	**-**	ns
t_{PDHL}	LGATE Turn-On Propagation Delay	V_{VCC} = 5V, outputs unloaded	**-**	20	**-**	ns
t_{PTS}	UG/LG Three-State Propagation Delay	V_{VCC} = 5V, outputs unloaded	-	35	-	ns
t_{LGMIN}	Minimum LG On-Time in DCM		-	350	-	ns
OUTPUT (Note 7)						
R_U	Upper Drive Source Resistance	500mA source current	-	1	**2.5**	Ω
I_U	Upper Driver Source Current	$V_{UGATE-PHASE}$ = 2.5V	-	2.00	-	A
R_U	Upper Drive Sink Resistance	500mA sink current	-	1	**2.5**	Ω
I_U	Upper Driver Sink Current	$V_{UGATE-PHASE}$ = 2.5V	-	2.00	-	A
R_L	Lower Drive Source Resistance	500mA source current	-	1	**2.5**	Ω
I_L	Lower Driver Source Current	V_{LGATE} = 2.5V	-	2.00	-	A
R_L	Lower Drive Sink Resistance	500mA sink current	-	0.5	**1.0**	Ω
I_L	Lower Driver Sink Current	V_{LGATE} = 2.5V	-	4.00	-	A

NOTES:

7. Limits established by characterization and are not production tested.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Application With 2-Phase Converter

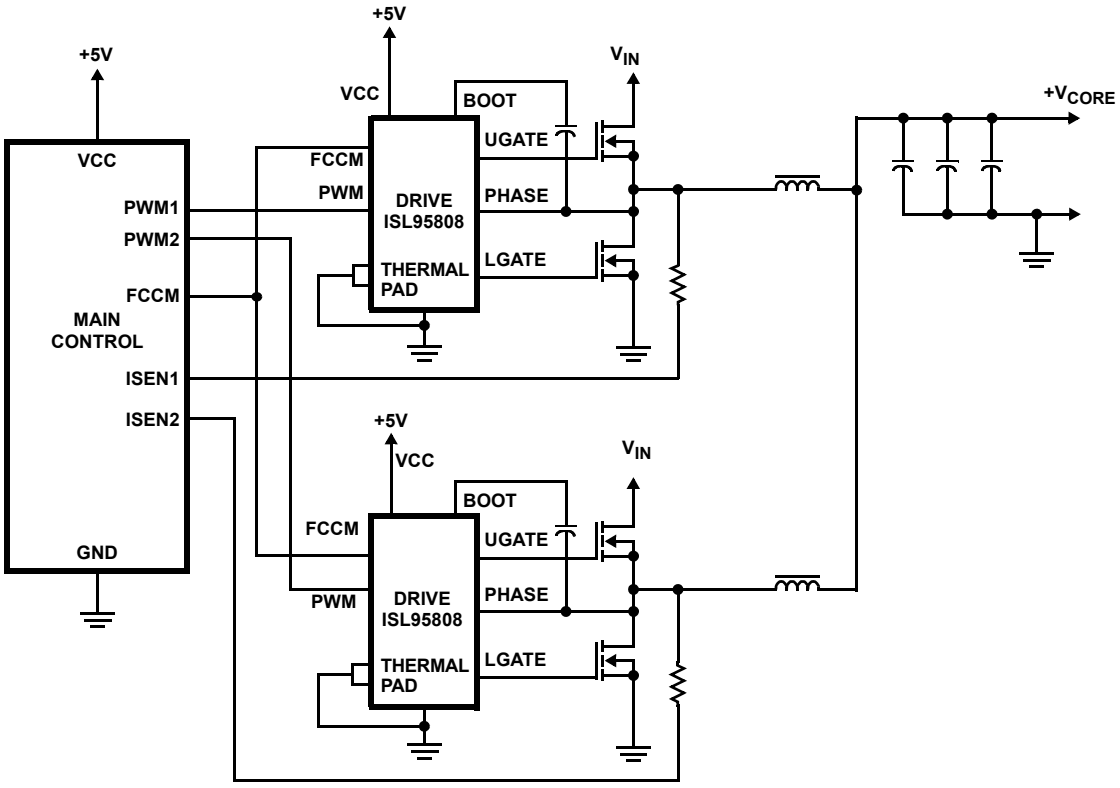


FIGURE 2. TYPICAL APPLICATION WITH 2-PHASE CONVERTER

PS4 Exit Timing Diagram

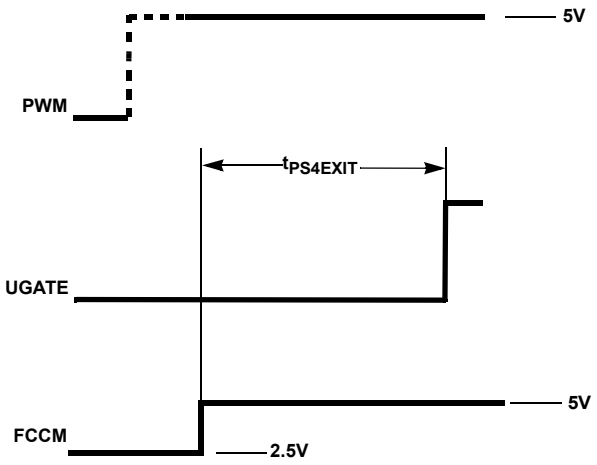


FIGURE 3. PS4 EXIT TIMING DIAGRAM

Timing Diagram

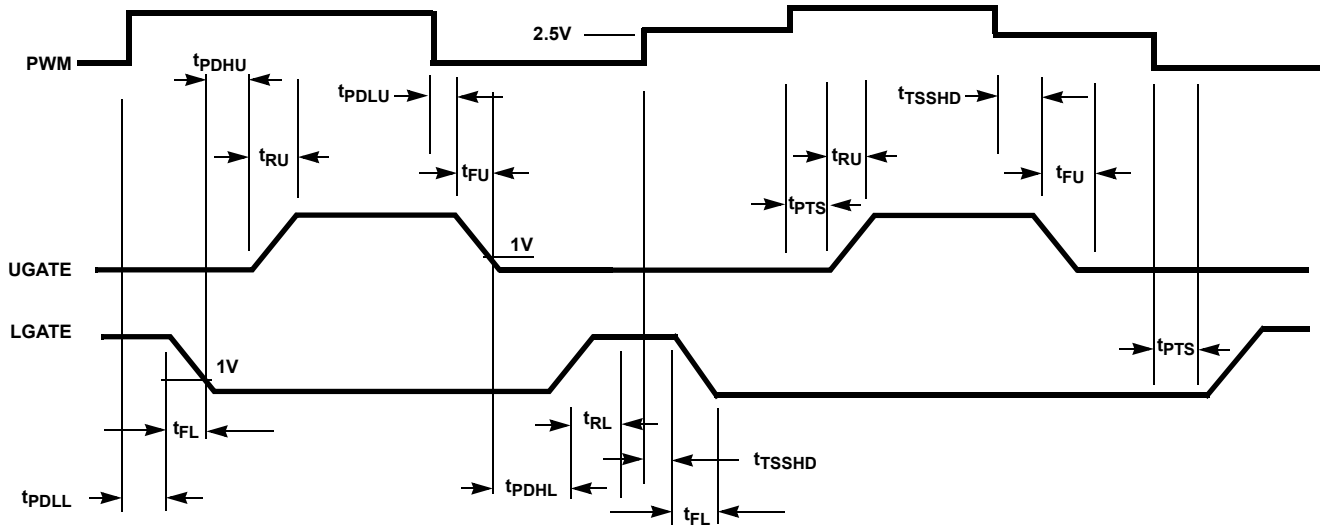


FIGURE 4. TIMING DIAGRAM

Description

Theory of Operation

Designed for speed, the ISL95808 dual MOSFET driver controls both high-side and low-side N-Channel FETs from one externally provided PWM signal.

A rising edge on PWM initiates the turn-off of the lower MOSFET (see "Timing Diagram"in Figure 4). After a short propagation delay [t_{PDLL}], the lower gate begins to fall. Typical fall times [t_{FL}] are provided in the "Electrical Specifications" table on page 4. Adaptive shoot-through circuitry monitors the LGATE voltage. When LGATE has fallen below 1V, UGATE is allowed to turn on. This prevents both the lower and upper MOSFETs from conducting simultaneously, or shoot-through.

A falling transition on PWM indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay [t_{PDLU}] is encountered before the upper gate begins to fall [t_{FU}]. The upper MOSFET gate-to-source voltage is monitored and the lower gate is allowed to rise after the upper MOSFET gate-to-source voltage drops below 1V. The lower gate then rises [t_{RL}], turning on the lower MOSFET.

This driver is optimized for converters with large step-down compared to the upper MOSFET because the lower MOSFET conducts for a much longer time in a switching period. The lower gate driver is therefore sized much larger to meet this application requirement.

The 0.5Ω ON-resistance and 4A sink current capability enables the lower gate driver to absorb the current injected to the lower gate through the drain-to-gate capacitor of the lower MOSFET. This prevents a shoot-through caused by the high dv/dt of the phase node.

The PWM and FCCM pins actively pull to mid-supply if left OPEN.

Diode Emulation

Diode emulation allows for higher converter efficiency under light load situations. With diode emulation active, the ISL95808 will detect the zero current crossing of the output inductor and turn off LGATE. This ensures that Discontinuous Conduction Mode (DCM) is achieved. Diode emulation is asynchronous to the PWM signal. Therefore, the ISL95808 will respond to the FCCM input immediately after it changes state.

NOTE: Intersil does not recommend diode emulation use with $r_{DS(ON)}$ current sensing topologies. The turn-off of the low-side MOSFET can cause gross current measurement inaccuracies.

Three-State PWM Input

A unique feature of the ISL95808 and other Intersil drivers is the addition of a shutdown window to the PWM input. If the PWM signal enters and remains within the shutdown window for a set hold-off time, the output drivers are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. Otherwise, the PWM rising and falling thresholds outlined in the "Electrical Specifications" table on page 3 determine when the lower and upper gates are enabled.

The VCC pin of the driver(s) and related VCC or +5V bias supply pin of the Intersil controller must share a common +5V supply.

Adaptive Shoot-Through Protection

Both drivers incorporate adaptive shoot-through protection to prevent upper and lower MOSFETs from conducting simultaneously and shorting the input supply. This is accomplished by ensuring the falling gate has turned off one MOSFET before the other is allowed to turn on.

During turn-off of the lower MOSFET, the LGATE voltage is monitored until it reaches a 1V threshold, at which time the UGATE is released to rise. Adaptive shoot-through circuitry monitors the upper MOSFET gate-to-source voltage during UGATE turn-off. Once the upper

MOSFET gate-to-source voltage has dropped below a threshold of 1V, the LGATE is allowed to rise.

Internal Bootstrap Diode

This driver features an internal bootstrap Schottky diode. Simply adding an external capacitor across the Boot and Phase pins completes the bootstrap circuit.

The bootstrap capacitor must have a maximum voltage rating above the maximum battery voltage plus 5V. The bootstrap capacitor can be derived from Equation 1:

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V_{BOOT}} \quad \text{(EQ. 1)}$$

Where Q_{GATE} is the amount of gate charge required to fully charge the gate of the upper MOSFET. The ΔV_{BOOT} term is defined as the allowable droop in the rail of the upper drive.

As an example, suppose an upper MOSFET has a gate charge, Q_{GATE}, of 25nC at 5V and also assume the droop in the drive voltage over a PWM cycle is 200mV. One will find that a bootstrap capacitance of at least 0.125µF is required. The next larger standard value capacitance is 0.15µF. A good quality ceramic capacitor is recommended.

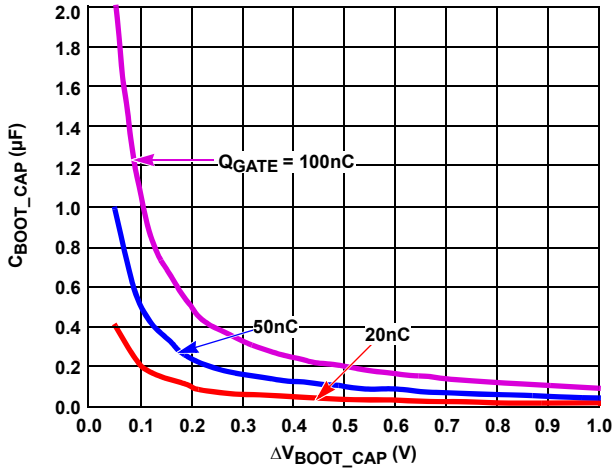


FIGURE 5. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

Power Dissipation

Package power dissipation is mainly a function of the switching frequency and total gate charge of the selected MOSFETs. Calculating the power dissipation in the driver for a desired application is critical to ensuring safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of +125°C. When designing the driver into an application, it is recommended that the following calculation be performed to ensure safe operation at the desired frequency for the selected MOSFETs. The power dissipated by the driver is approximated, as shown in Equation 2:

$$P = f_{SW}(1.5V_U Q_U + V_L Q_L) + I_{VCC} V_{CC} \quad \text{(EQ. 2)}$$

Where f_{SW} is the switching frequency of the PWM signal. V_U and V_L represent the upper and lower gate rail voltage. Q_U and Q_L is the upper and lower gate charge determined by MOSFET selection and any external capacitance added to the gate pins. The IV_{CC} V_{CC} product is the quiescent power of the driver and is typically negligible.

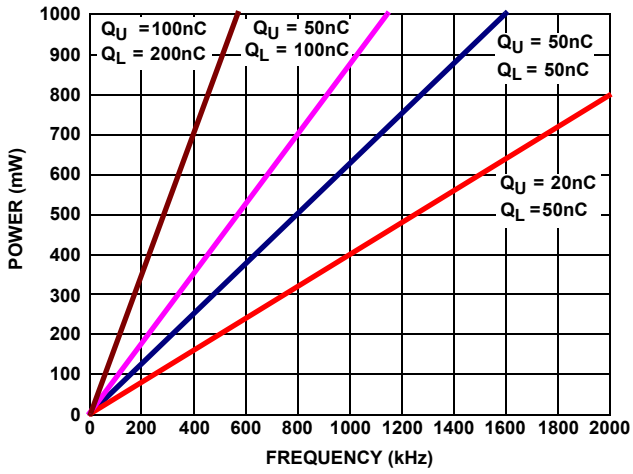


FIGURE 6. POWER DISSIPATION vs FREQUENCY

Layout Considerations

Reducing Phase Ring

The parasitic inductances of the PCB and power devices (both upper and lower FETs) could cause increased PHASE ringing, which may lead to voltages that exceed the absolute maximum rating of the devices. When PHASE rings below ground, the negative voltage could add charge to the bootstrap capacitor through the internal bootstrap diode. Under worst-case conditions, the added charge could overstress the Boot and/or Phase pins. To prevent this from happening, the user should perform a careful layout inspection to reduce trace inductances, and select low lead inductance MOSFETs and drivers. D^2PAK and DPAK packaged MOSFETs have high parasitic lead inductances. If higher inductance MOSFETs must be used, a Schottky diode is recommended across the lower MOSFET to clamp negative phase ring.

A good layout would help reduce the ringing on the phase and gate nodes significantly:

- Avoid using vias for decoupling components where possible, especially in the Boot-to-Phase path. Little or no use of vias for VCC and GND is also recommended. Decoupling loops should be short.
- All power traces (UGATE, PHASE, LGATE, GND and VCC) should be short and wide, and avoid using vias. If vias must be used, two or more vias per layer transition is recommended.
- Keep the SOURCE of the upper FET as close as thermally possible to the DRAIN of the lower FET.
- Keep the connection in between the SOURCE of lower FET and power ground wide and short.
- Input capacitors should be placed as close to the DRAIN of the upper FET and the SOURCE of the lower FET as thermally possible.

Refer to Tech Brief TB447 “Guidelines for Preventing Boot-to-Phase Stress on Half-Bridge MOSFET Driver ICs” for more information.

FCCM Trace Placement

FCCM trace should not be placed next to digital signal traces or PWM/PHASE traces from other channels in multiphase designs.

Thermal Management

For maximum thermal performance in high current, high switching frequency applications, connecting the thermal pad of the DFN part to the power ground with multiple vias is recommended. This heat spreading allows the part to achieve its full thermal potential.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
May 25, 2016	FN8689.2	Additional information added on page 2 and page 6 relative to +5V supply being common between VCC of ISL95808 and Intersil controllers. On page 3 added AC rating for the Boot pin to existing DC rating.
June 29, 2015	FN8689.1	Removed additional information from DFN package bullet listed in features on page 1. Ordering Information Table on page 2 changed to reflect addition of IRZ rated product and updated product markings. Part marking updated for HRZ version. Electrical Spec table beginning on page 3 updated to reflect IRZ addition. Changed MIN value of “Forward Voltage” on page 3 from 0.50 to 0.43 Updated POD L8.2x2D with current version, changes are as follows: Tiebar Note 5 updated From: "Tiebar shown (if present) is a non-functional feature." To: "Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends)."
October 24, 2014	FN8689.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

© Copyright Intersil Americas LLC 2014-2016. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

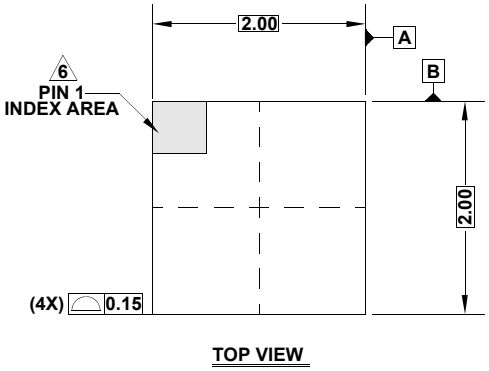
For information regarding Intersil Corporation and its products, see www.intersil.com

Package Outline Drawing

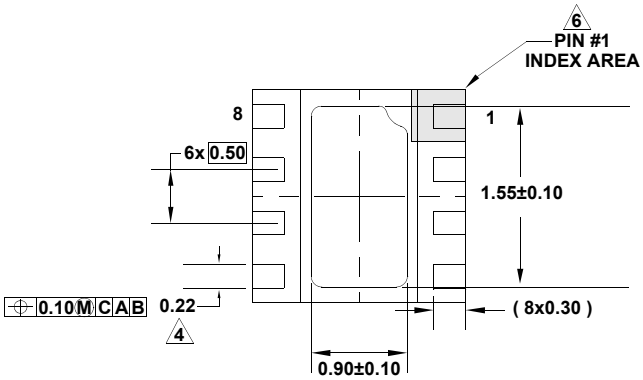
L8.2x2D

8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE (DFN) WITH EXPOSED PAD

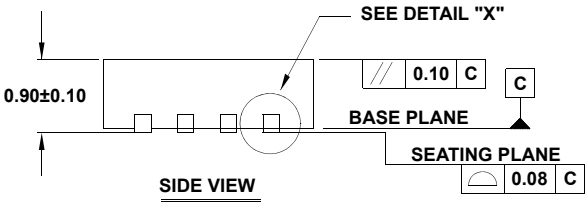
Rev 1, 3/15



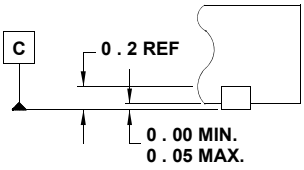
TOP VIEW



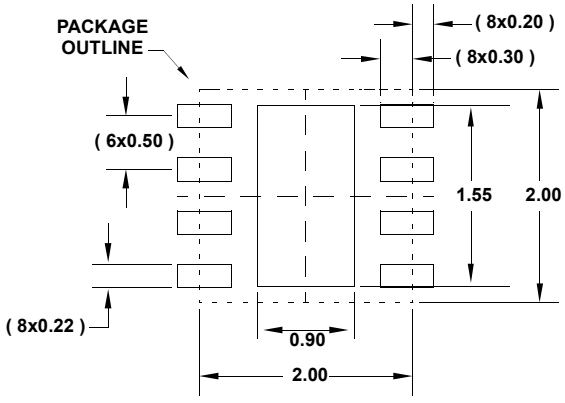
BOTTOM VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.