Non Isolated Buck Type Power Factor Correction LED Constant Current Driver Circuit

1. General Description

CS9220S is a source power factor correction high precision non isolated buck type LED constant current driver circuit for 85Vac~265Vac universal input voltage range. This driver IC integrated source power factor corrective circuit to realize high power correction factor and low distortion.

With unique sampling and constant current control method, output current of CS9220S can be controlled within +/-3%. Voltage/ load adjust ratio, and safety operation temperature control are main characteristics of CS9220S.

Complete protection functions are providing by CS9220S including LED open/short circuit protection, current limitation, inductance short circuit and it is auto reboot after all functions. The unique over temperature detection adjust reduces the output current to protect both power and load when high system temperature detected. Also, the imbedded soft start circuit reduced the stress of LED when light is turn on and off.

CS9220S with excellent current control capability is majorly applied for the LED lighting.

Features

500V Power MOSFET Inside
+/-3% LED output current precision
High PF (>0.9)
LLC control mode
Excellent Linear / Load Adjustment Ratio
Excellent current/temperature compensation
High Efficiency (> 90%)
Soft start
LED Open/Short Protection
Chip Over Temperature Protection
Assembly: SOP8

2. Function Diagram and Lead

2.1 Function Diagram

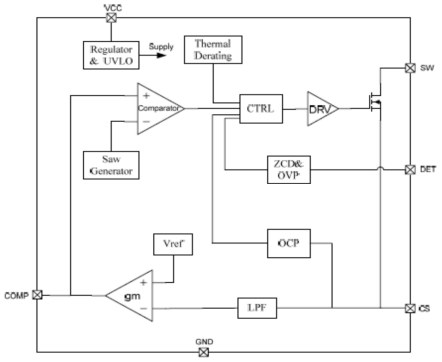


Fig 1 Function Diagram

2.2 Descriptions

CS9220S is operated by LLC mode and thus with small EMI(dv/dt) and heat generation to help for design space reduce. Also, chip is able to with the characteristics of good linear/load/temperature adjust ratio without compensation from outside. The imbedded PFC control mechanism helps for system power correction factor above 0.9. CS9220S integrated functions of LED open/short protection, inductance short circuit and over temperature protection. Imbedded soft start reduced the over current stress when LED turn on.

2.2.1 Power-on

When system power on, line voltage charges Vcc capacitor through turn on current limitation resistor. As Vcc up to the turn-on voltage, CS9220S begin to provide pulse signal to transfer the input energy out through inductance and the output voltage begin to rise to charge Vcc when output voltage over Vcc.

The bandwidth is narrow in PFC control traditionally to lead for the long turn-on time and high output energy stress. CS9220S by unique dynamic control can prevent overvoltage adjust and realized fast turn-on in LED.

2.2.2 Fix conduction duration and LLC control model

CS9220S by fix duration for conduction control, inductance current with similar shape of sine wave and follows the phase of input AC voltage to realize higher power correction factor. Because CS9220S by buck topology structure design, no output when input voltage lowers than LED will diminish power correction factor. Limitation of output voltage is suggested when real application. Also LED light voltage is suggested to controlled below 75V when input voltage by 85~265Vac universal range.

CS9220S is taking LLC control model, inductance will resonance with parasitic capacitance in switch drain when inductance current drop to zero. The chip will not open MOSFET before lowest resonance detected to prevent damage.

2.2.3 Output current setting

CS9220S by unique current sampling and constant current control mechanism is able to realize high precision current for LED. The output current calculation follows by

$$I_{OUT} = \frac{V_{ref}}{R_{CS}}$$

Vref is internal reference voltage, typical voltage is 200mV

Rcs is resistance of current sampling resistor

2.2.4 Feedback

CS9220S detect inductance current through DET pin also for over voltage protection. The over voltage protection threshold is 4.0V and the ratio of voltage divider resistances can set to

$$\frac{R_{DET\_L}}{R_{DET\_L} + R_{DET\_H}} = \frac{4.0}{V_{OVP}}$$

R_{DET_L} is lower voltage divider resistance

R_{DET_H} is higher voltage divider resistance

V_{OVP} is the output voltage protection setting

2.2.5 Protection

CS9220S provide full range protections including LED open/short, low input voltage, current limitation, inductance short and over temperature.

When LED open, DET voltage rises with the output voltage. Chip will stop the switch when continuous 3 cycles DET voltage over threshold.

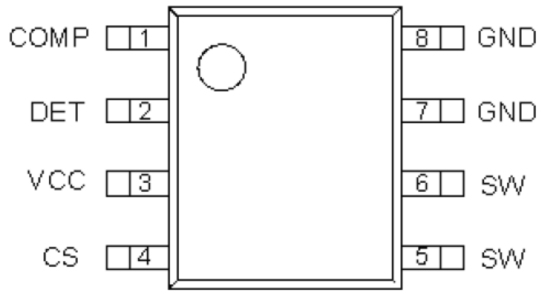
When LED short, system operation frequency is 20kHz, CS is clamped at 0.5V to reduce the power loss. During the short circuit, the inductance energy diminishes by charging Vcc and system saturation when Vcc voltage drops.

When inductance short, current rise rapidly when switch been turn on. Detecting circuit will turn off the switch to protect whole circuit when voltage of pin CS over voltage protection threshold.

When chip junction temperature reaches the setting of over temperature protection, over heat adjust function in chip will be triggered to lower system output current and prevent both chip and system from been over heat damage.

During protection function startup period, system will keep tracking the status and recovered if cleaning of abnormal signals.

2.3 Pin Diagram



2.4 pin Function

Pin Name	Pin #	Function
COMP	1	Loop compensate pin
DET	2	Feedback sense pin
Vcc	3	Chip power source pin
CS	4	Current sense pin
SW	5,6	Power Switch
GND	7,8	Chip Ground

3 Electrical Characteristics

3.1 Limit operation conditions

Unless specified, all parameter is note by Tamb=25 ^{o}C

Symbol	Parameter	limit	Unit
V_{sw_MAX}	Max SW operation voltage	500	V
V_{CC}	Max Vcc operation voltage	24	V
V_{CC_clamp}	Max Vcc clamping voltage	28	V
I_{CC_clamp}	Max Vcc clamping current	10	mA
I_{DET_MAX}	Max DET current	-50~10	mA
V_{CS}	Vcs voltage	-0.3~24	V
$V_{I/O}$	Other pin I/O voltage	-0.3~7	V
T_{OPT}	Operation temperature range	-40~125	^{o}C
T_{STG}	Max/Min storage temperature	-55~150	^{o}C
Rthja	Thermal resistance junction to ambient	184	^{o}C /W
HBM	ESD(Human Body Mode) Note 2	2	kV
V_{VCC}	Power voltage	10~24	V
T_{OPT}	Max/Min operation ambient temperature	-40~85	^{o}C

Note 1 over limit use of CS9220S may lead to device permanent damage.

Note 2 ESD Human body mode, 100pF capacitor discharge through 1.5K-ohm resistor

3.2 Electrical parameters

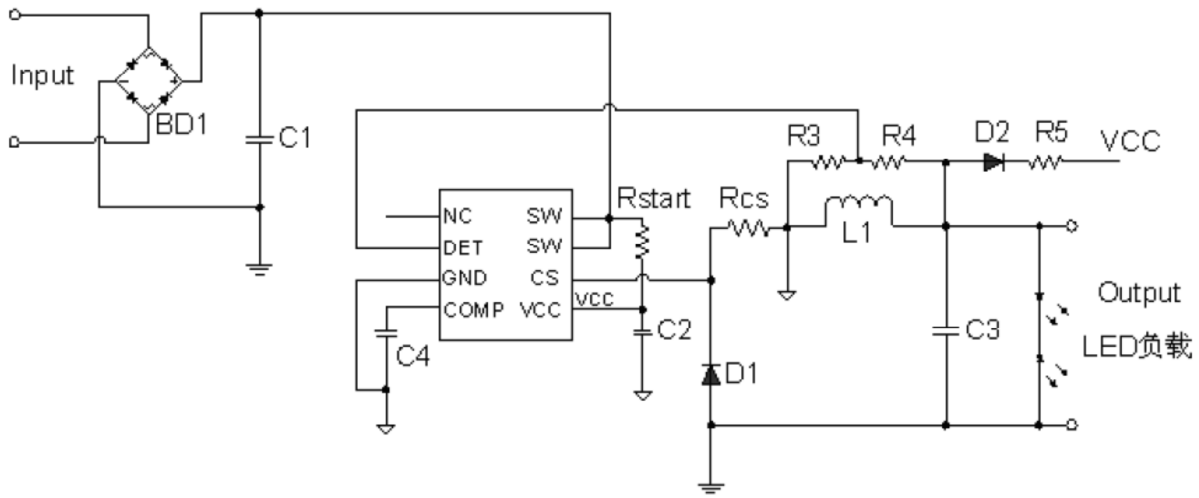
Unless specified, VCC=14V, Tamb=25 ^{o}C

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
Power source						
V_{CC_ON}	Turn-on voltage	V_{CC} rise	16.2	18	19.8	V
V_{CC_OFF}	V_{CC} turn-off voltage	V_{CC} down	7.5	8.5	9.5	V
V_{CC_Clamp}	V_{CC} Clamp	I_{CC} =10mA		28		V
$I_{Startup}$	V_{CC} startup current	V_{CC}=15V		35	80	mA
I_{VCC_Quiet}	V_{CC} operation current (no switch on/off)			0.36	0.7	mA
I_{VCC_OPER}	V_{CC} operation current (switch on/off)	F_{GATE_AVG}=50KHz, C_{GATE}=0.47nF		0.6	1	mA
Error Amplifier						
V_{Ref}	Internal reference		0.194	0.2	0.206	V

	voltage					
V_{COMP_RANG}	COMP voltage range		0.8		2.5	V
G_{EA}	EA			35		uA/V
Current Sampling						
T_{LEB}	Lead edge Blanking time			280		nS
V_{CS_Clamp}	CS clamp voltage		0.94	1	1.06	V
V_{CS_Prot}	CS over current protection voltage Threshold			2.5		V
DET Feedback						
V_{ZCD}	Zero current detection voltage threshold			0		V
V_{ZCD_H}	Zero current detection voltage delay			1.4		V
V_{DET_OVP}	Over voltage protection threshold		3.6	4	4.4	V
T_{ON_MAX}	Max conduction time			15		uS
T_{OFF_MIN}	Minimum off time			5		uS
T_{Start}	Time for counter start	V_{DET}<0.35V		50		uS
Power MOSFET						
V_{DS_BD}	MOSFET breakdown voltage	Vgs=0V/Id=250uA	500			V
Idss	Leakage current	Vgs=0V/Vds=500V			1	uA

R_{DSON}	Conduction resistance	V_{GS}=10V/Id=1A		5	9	ohm
Over temperature protection						
T_{REG}	Over temperature setting			130		^{o}C
T_{OTP}	Over temperature protection			150		^{o}C

4. Typical Application Diagram



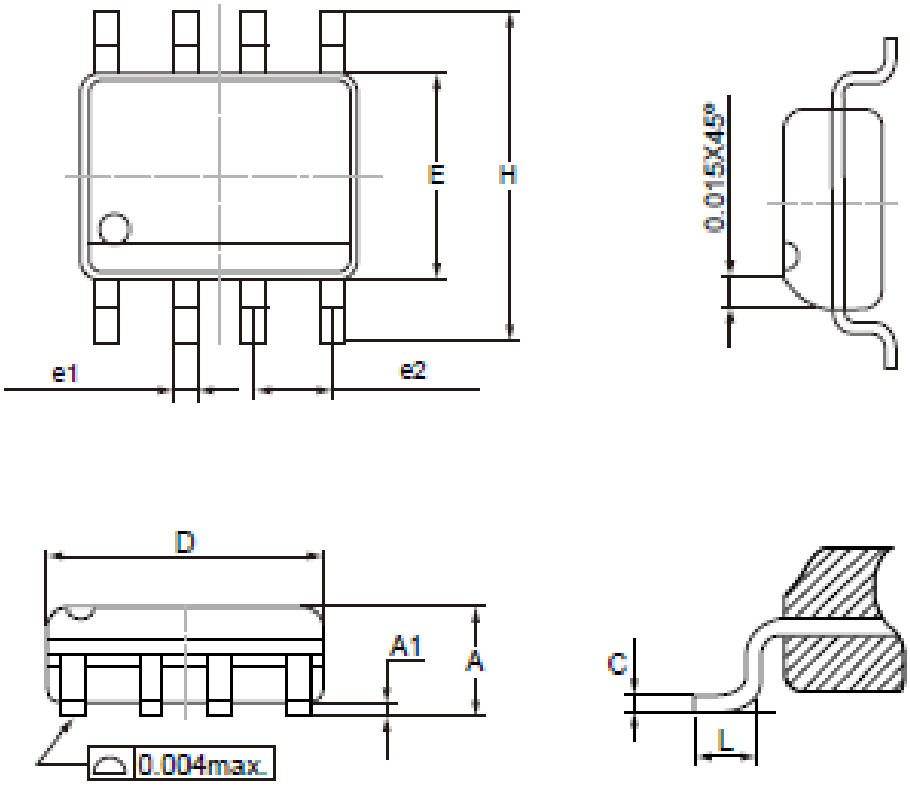
***Notice for PCB Layout**

Following suggestion should be noted for CS9220S in PCB design

1. Minimum circuit area is suggest to minimize EMI
2. Capacitor (C2/C4) should arranged as close to VCC and COMP pin as possible
3. Current sampling resistor ground line should be as short as possible and close to VCC capacitor/chip ground.
4. Voltage divider resistor (R3/R4) need to close to DET
5. Heat sink at SW will help for heat dissipation

5. Package Outline and Dimension

SOP-8 Packaging Outline



SYMBOLS	Millimeters			Inches		
	MIN.	Nom.	MAX.	MIN.	Nom.	MAX.
A	1.35	1.55	1.75	0.053	0.061	0.069
A1	0.10	0.17	0.25	0.004	0.007	0.010
C	0.18	0.22	0.25	0.007	0.009	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	3.80	3.90	4.00	0.150	0.154	0.158
H	5.80	6.00	6.20	0.229	0.236	0.244
e1	0.35	0.43	0.56	0.014	0.017	0.022
e2	1.27BSC			0.05BSC		
L	0.40	0.65	1.27	0.016	0.026	0.050