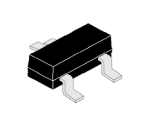
P-Channel Power MOSFET

CDM5203



SOT-23

SOT-23
Surface Mount
Plastic Package
RoHS compliant

GENERAL DISCRIPTION:

These P-channel MOSFETs utilize advanced processing techniques to achieve the extremely low on-resistance per silicon area. This benefit provides the designer with an extremely efficient device for use in battery and load management applications.

A thermally enhanced large pad lead frame has been incorporated into the standard SOT-23 package to produce a HEXFET Power MOSFET with the industry's smallest footprint. This package, dubbed the Micro3^{TM},is ideal for applications where printed circuit board space is at a premium. The low profile (<1.1mm) of the Micro3 allows it to fit easily into extremely thin application environments such as portable electronics and PCMCIA cards. The thermal resistance and power dissipation are the best available.

FEATURE

1. Ultra Low On-Resistance
2. P-Channel MOSFET
3. Surface Mount
4. Available in Tape & Reel
5. Low Gate Charge
6. Lead-Free
7. Halogen-Free

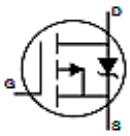
ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Parameter	SYMBOL	VALUE	UNIT
Drain- Source Voltage	V_{DS}	30	V
Continuous Drain Current, V_{GS} @ 10V @ T_A = 25°C	I_D	3.0	A
Continuous Drain Current, V_{GS} @ 10V T_A= 70°C	I_D	2.4	A
Pulsed Drain Current [1]	I_{DM}	24	A
Power Dissipation @T_A = 25°C	P_D	1.25	W
Power Dissipation @T_A = 70°C	P_D	0.80	W
Linear Derating Factor		10	mW/°C
Gate-to-Source Voltage	V_{GS}	±20	V
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

THERMAL RESISTANCE

Maximum Junction-to-Ambient [3]	$R_{\theta JA}$	100	°C/W

ELECTRICAL CHARACTERISTICS at T_a = 25 °C

Parameter	Symbol	Test Condition	Value			Unit
			Min	Typ.	Max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	30	--	--	V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to 25°C, I_D = 1mA	--	0.019	--	V/°C
Static Drain-to-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = 3.0A [2]	--	--	98	mΩ
		V_{GS} = -4.5V, I_D = 2.6A [2]	--	--	165	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.0	--	2.5	V
Forward Transconductance	gfs	V_{DS} = -10V, I_D = 3.0A	3.1	--	--	S
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V	--	--	1.0	μA
		V_{DS} = 24V, V_{GS} = 0V, T_J = 70°C	--	--	5.0	
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS} = 20V	--	--	100	nA
Gate-to-Source Reverse Leakage		V_{GS} = 20V	--	--	100	
Total Gate Charge	Q_g	I_D = 3.0A	--	9.5	14	nC
Gate-to-Source Charge	Q_{gs}	V_{DS} = 24V	--	2.3	3.5	
Gate-to-Drain ("Miller") Charge	Q_{gd}	V_{GS} = 10V [2]	--	1.6	2.4	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15V [2]	--	12	--	ns
Rise Time	t_r	I_D = 1.0A	--	18	--	
Turn-Off Delay Time	$t_{d(off)}$	R_G = 6.0Ω	--	88	--	
Fall Time	t_f	V_{GS} = 10V	--	52	--	
Input Capacitance	C_{iss}	V_{GS} = 0V	--	510	--	pF
Output Capacitance	C_{oss}	V_{DS} = 25V	--	71	--	
Reverse Transfer Capacitance	C_{rss}	f = 1.0MHz	--	43	--	
Source-Drain Ratings and Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode 	--	--	1.3	A
Pulsed Source Current (Body Diode) [1]	I_{SM}		--	--	24	
Diode Forward Voltage	V_{SD}	T_J = 25°C, I_S = -1.3A, V_{GS} = 0V [2]	--	--	1.2	V
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = 1.3A	--	17	26	ns
Reverse Recovery Charge	Q_{rr}	di/dt = -100A/μs [2]	--	12	18	nC

Note:

1. Repetitive rating; pulse width limited by max. junction temperature
2. Pulse width ≤ 400μs; duty cycle ≤ 2%
3. Surface mounted on FR-4 board, t ≤ 5sec
4. For PNP device voltage and current values will be negative (-).

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

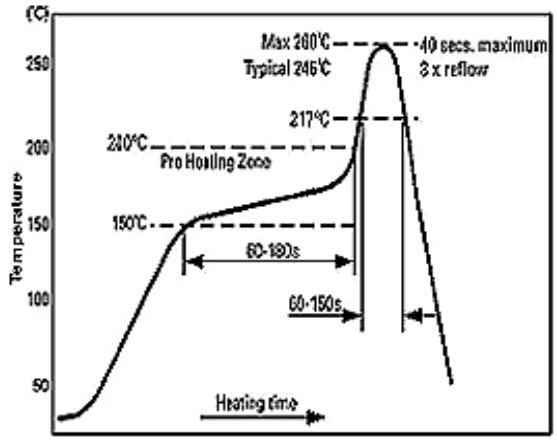
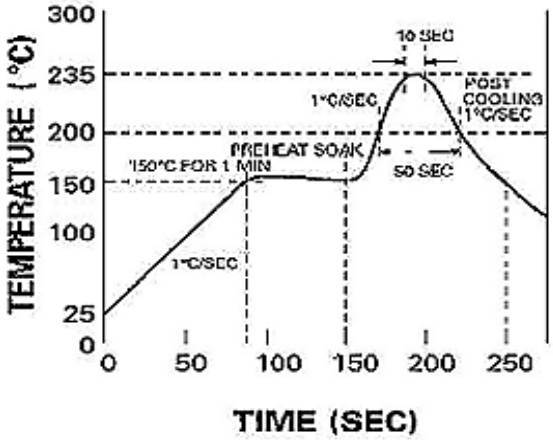


Figure 2

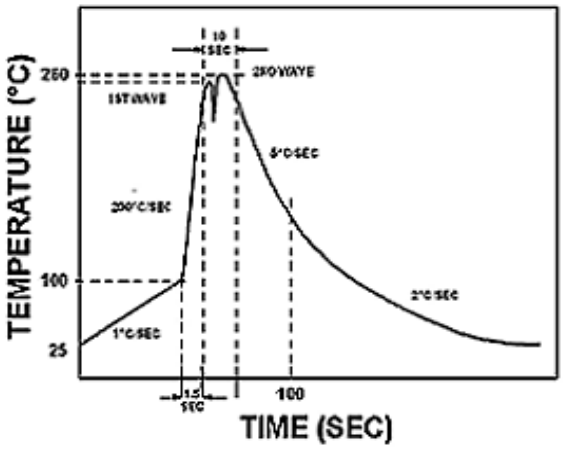


Reflow profiles in tabular form

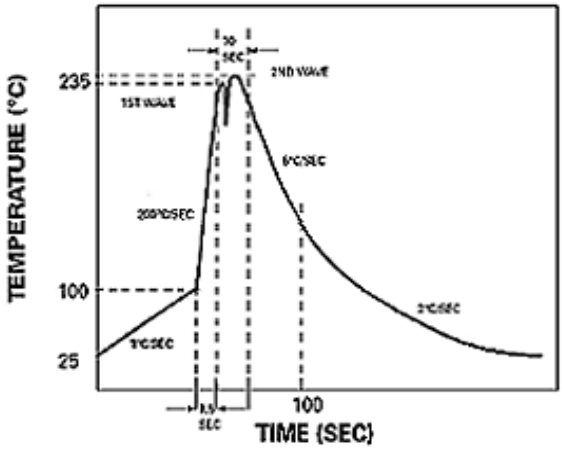
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	150-170°C 60-180 seconds	150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	200°C 30-50 seconds	217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder

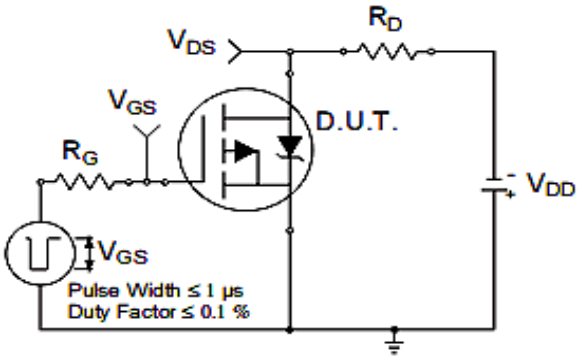


Wave Profiles in Tabular Form

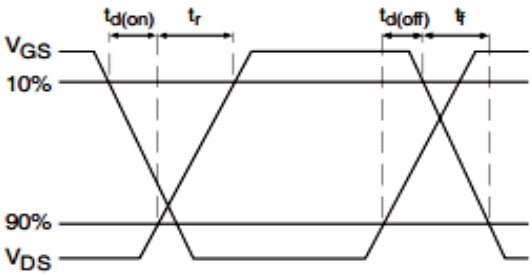
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

TEST CIRCUIT AND DIAGRAMS

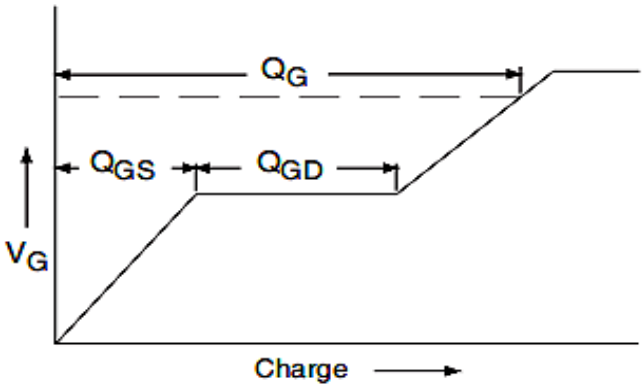
Switching Time Test Circuit



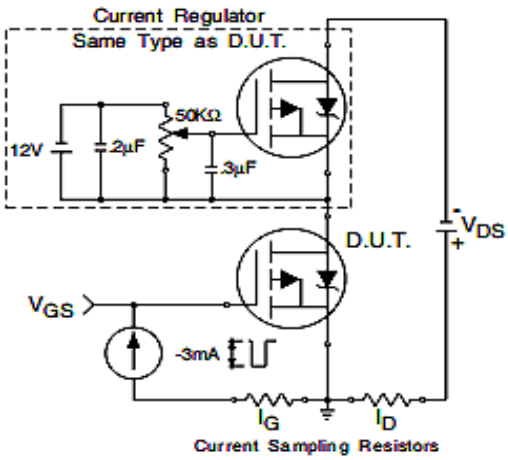
Switching Time Waveforms



Basic Gate Charge Waveform



Gate Charge Test Circuit



Typical Characteristic Curves

Fig 1: Typical Output Characteristics

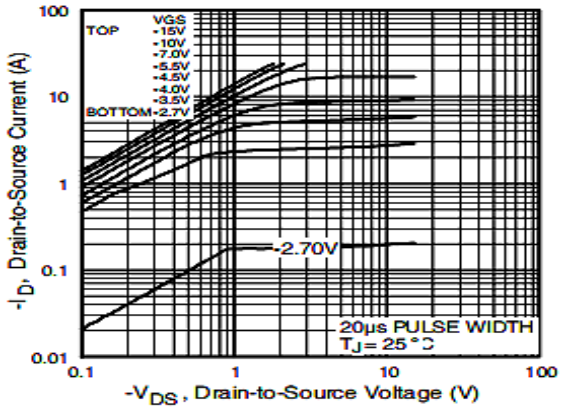


Fig 2: Typical Transfer Characteristics

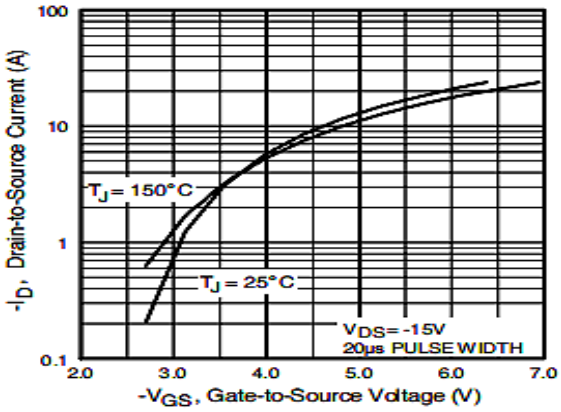


Figure 3: Typical Capacitance Vs. Drain-to-Source Voltage

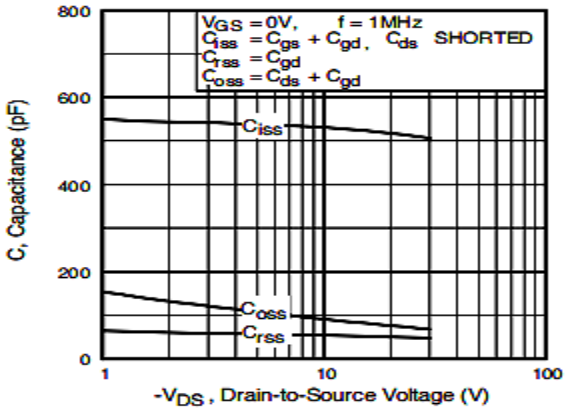


Fig 4: Typical Output Characteristics

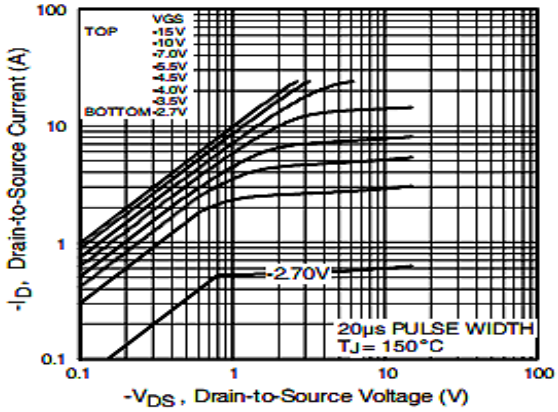


Fig 5: Normalized On-Resistance Vs. Temperature

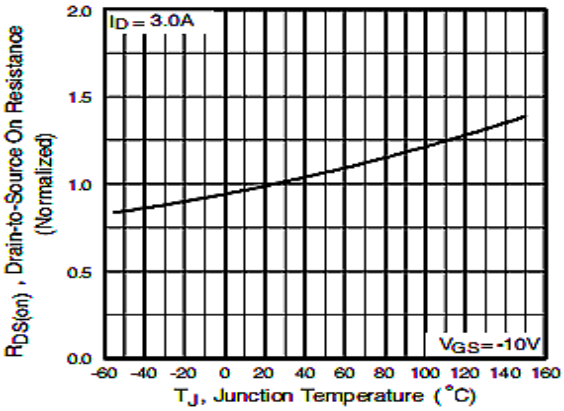
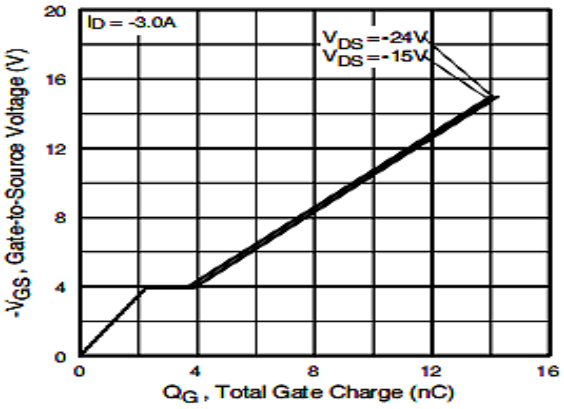


Figure 6: Typical Gate Charge Vs. Gate-to-Source Voltage



Typical Characteristic Curves

Figure 7. Typical Source-Drain Diode Forward Voltage

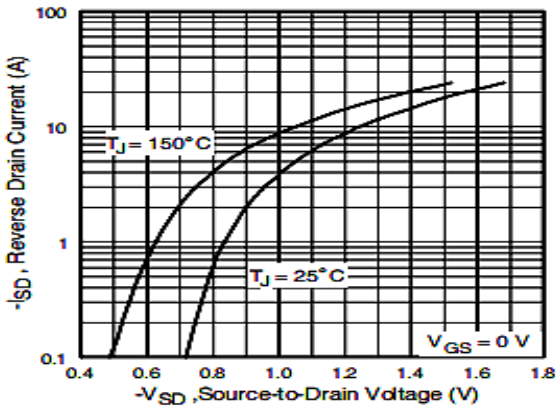


Fig 10: Maximum Safe Operating Area

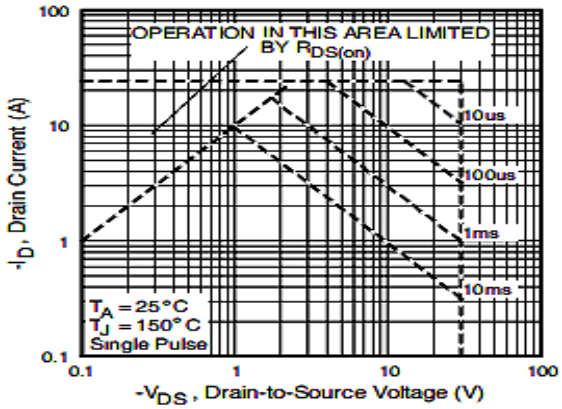


Figure 8: Typical On-Resistance Vs. Gate Voltage

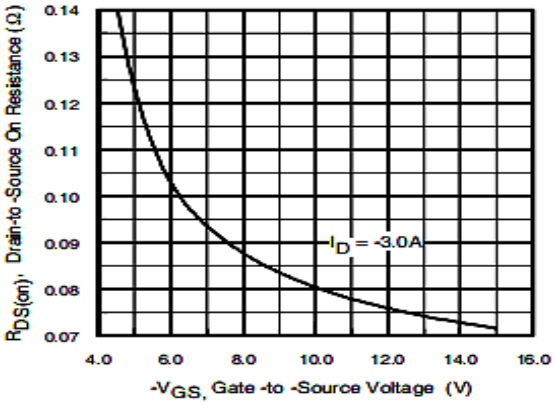


Fig 11: Typical On-Resistance Vs. Drain Current

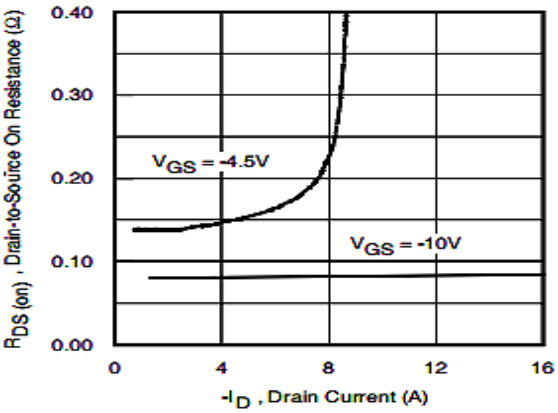


Fig 9: Threshold Voltage Vs. Temperature

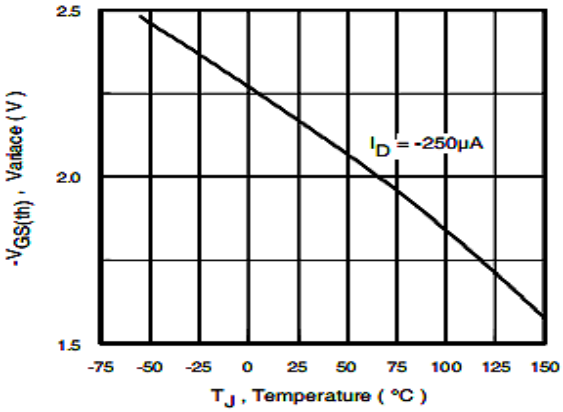
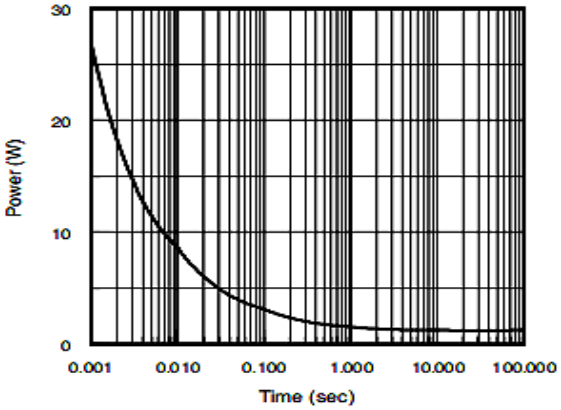


Fig 12: Typical Power Vs. Time



Typical Characteristic Curves

Fig 13: Maximum Drain Current Vs. Case Temperature

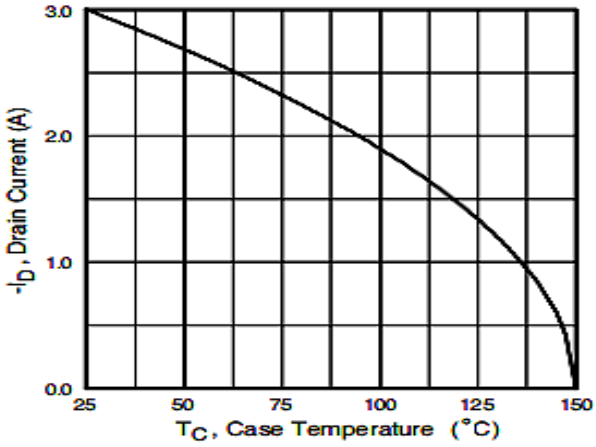
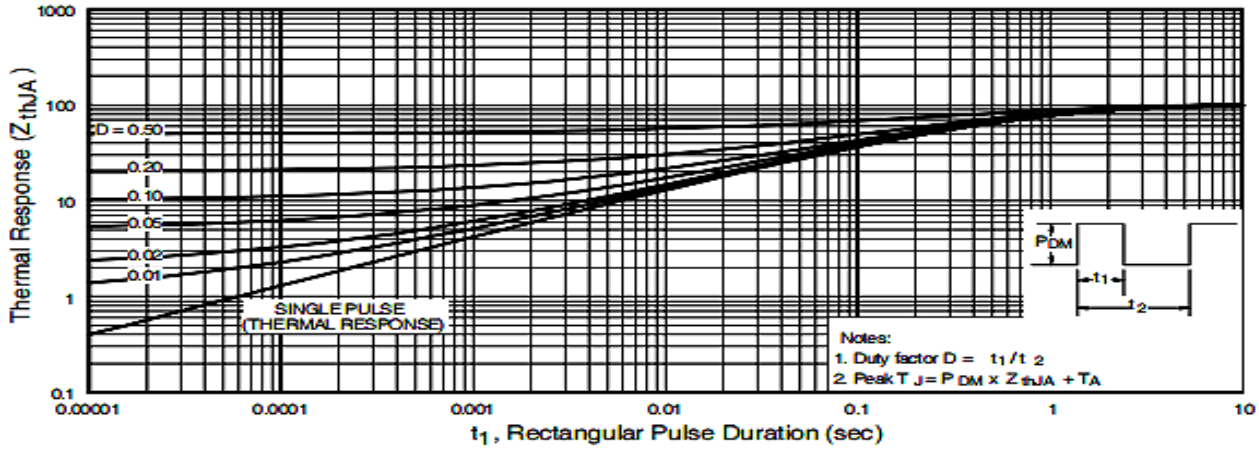
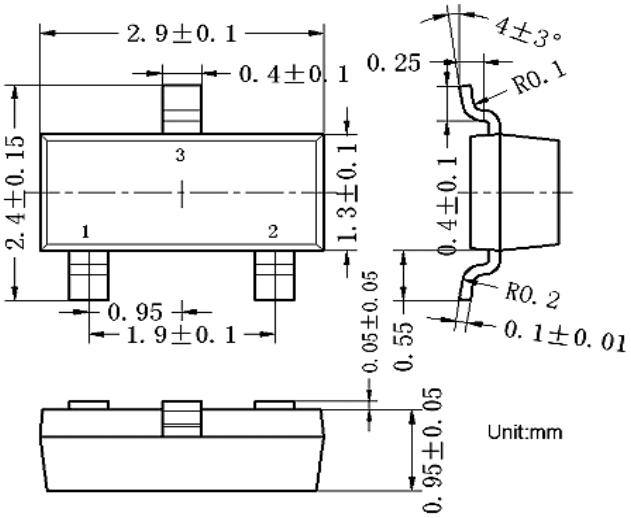


Fig 14: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



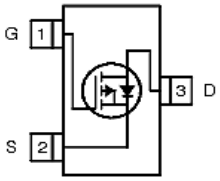
PACKAGE DETAILS

SOT-23 Formed SMD Package

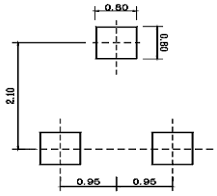


Pin configuration

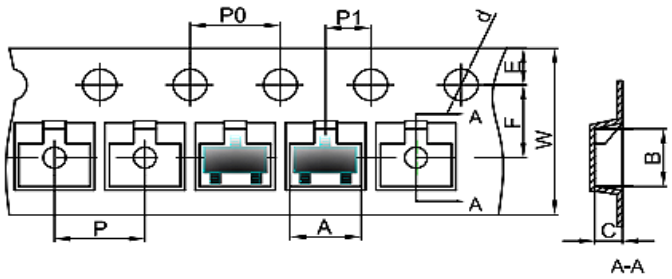
1. Gate
2. Source
3. Drain



Recommend PCB solder land [Unit: mm]



SOT-23 Embossed Carrier Tape

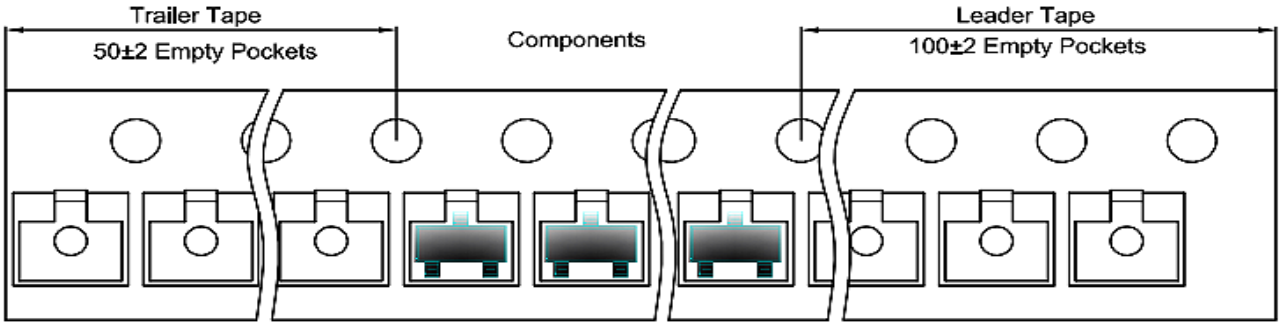


Packaging Description:

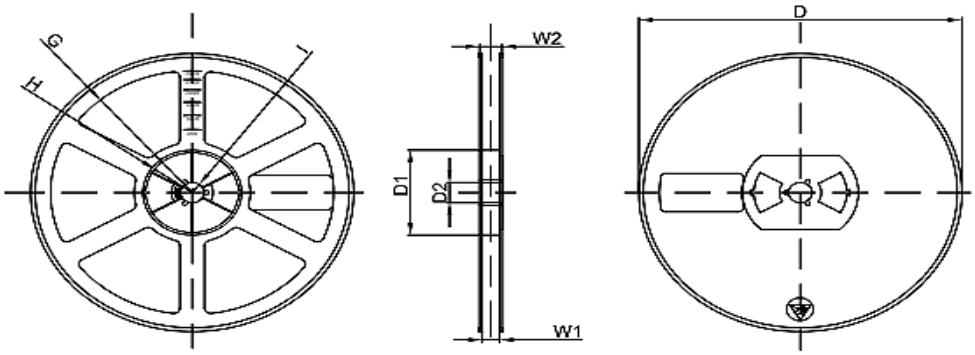
SOT-23 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 3,000 units per 7" or 17.8cm diameter reel. The reels are clear in color and is made of polystyrene plastic (anti-static coated).

Dimensions are in millimeter										
Pkg type	A	B	C	d	E	F	P0	P	P1	W
SOT-23	3.15	2.77	1.22	Ø1.50	1.75	3.50	4.00	4.00	2.00	8.00

SOT-23 TAPE LEADER & TRAILAR



SOT-23 REEL



Dimensions are in millimeter								
Reel Option	D	D1	D2	G	H	I	W1	W2
7"Dia	Ø178.00	54.40	13.00	R78.00	R25.60	R6.50	9.50	12.30

REEL	Reel Size	Box	Box Size(mm)	Carton	Carton Size(mm)	G.W.(kg)
3000 pcs	7 Inch	45,000 pcs	203×203×195	180,000 pcs	438×438×220	

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.

Floor Life

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH