# Precision Micropower, Low Dropout Voltage References

# REF19x Series

### FEATURES
**Initial Accuracy: ±2 mV Max**
**Temperature Coefficient: 5 ppm/°C Max**
**Low Supply Current: 45 μA Max**
**Sleep Mode: 15 μA Max**
**Low Dropout Voltage**
**Load Regulation: 4 ppm/mA**
**Line Regulation: 4 ppm/V**
**High Output Current: 30 mA**
**Short-Circuit Protection**

### APPLICATIONS
**Portable Instrumentation**
**A/D and D/A Converters**
**Smart Sensors**
**Solar Powered Applications**
**Loop Current Powered Instrumentations**

### GENERAL DESCRIPTION
The REF19x series precision band gap voltage references use a patented temperature drift curvature correction circuit and laser trimming of highly stable thin-film resistors to achieve a very low temperature coefficient and a high initial accuracy.

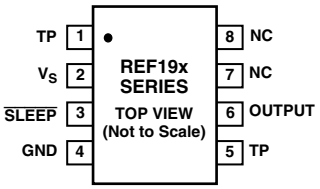
The REF19x series is made up of micropower, low dropout voltage (LDV) devices providing a stable output voltage from supplies as low as 100 mV above the output voltage and consuming less than 45 μA of supply current. In sleep mode, which is enabled by applying a low TTL or CMOS level to the $\overline{\text{SLEEP}}$ pin, the output is turned off and supply current is further reduced to less than 15 μA.

The REF19x series references are specified over the extended industrial temperature range (–40°C to +85°C) with typical performance specifications over –40°C to +125°C for applications such as automotive.

All electrical grades are available in 8-lead SOIC; the PDIP and TSSOP are available only in the lowest electrical grade. Products are also available in die form.

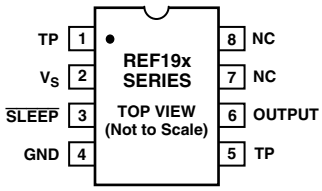
**Test Pins (TP)**
The test pins, Pin 1 and Pin 5, are reserved for in-package Zener-zap. To achieve the highest level of accuracy at the output, the Zener-zapping technique is used to trim the output voltage. Since each unit may require a different amount of adjustment, the resistance value at the test pins will vary widely from pin to pin as well as from part to part. The user should not make any physical or electrical connections to Pin 1 and Pin 5.

### PIN CONFIGURATIONS
**8-Lead SOIC and TSSOP**
**(S Suffix and RU Suffix)**




NC = NO CONNECT
TP PINS ARE FACTORY TEST POINTS, NO USER CONNECTION

**8-Lead PDIP (P Suffix)**




NC = NO CONNECT
TP PINS ARE FACTORY TEST POINTS, NO USER CONNECTION

**Table I.**

| Part Number | Nominal Output Voltage (V) |
|---|---|
| REF191 | 2.048 |
| REF192 | 2.50 |
| REF193 | 3.00 |
| REF194 | 4.50 |
| REF195 | 5.00 |
| REF196 | 3.30 |
| REF198 | 4.096 |

REV. F

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# REF191–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 3.3 V, $T_A$ = 25°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INITIAL ACCURACY[1] | | | | | | |
| E Grade | $V_O$ | $I_{OUT}$ = 0 mA | 2.046 | 2.048 | 2.050 | V |
| F Grade | | | 2.043 | | 2.053 | V |
| G Grade | | | 2.038 | | 2.058 | V |
| LINE REGULATION[2] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{IN}$ | 3.0 V ≤ $V_S$ ≤ 15 V, $I_{OUT}$ = 0 mA | | 2 | 4 | ppm/V |
| F and G Grades | | | | 4 | 8 | ppm/V |
| LOAD REGULATION[2] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S$ = 5.0 V, 0 mA ≤ $I_{OUT}$ ≤ 30 mA | | 4 | 10 | ppm/mA |
| F and G Grades | | | | 6 | 15 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S$ = 3.15 V, $I_{LOAD}$ = 2 mA | | | 0.95 | V |
| | | $V_S$ = 3.3 V, $I_{LOAD}$ = 10 mA | | | 1.25 | V |
| | | $V_S$ = 3.6 V, $I_{LOAD}$ = 30 mA | | | 1.55 | V |
| LONG-TERM STABILITY[3] | $DV_O$ | 1,000 Hours @ 125°C | | 1.2 | | mV |
| NOISE VOLTAGE | $e_N$ | 0.1 Hz to 10 Hz | | 20 | | µV p-p |

NOTES
[1]Initial accuracy includes temperature hysteresis effect.
[2]Line and load regulation specifications include the effect of self-heating.
[3]Long-term drift is guaranteed by 1,000 hours life test performed on three independent wafer lots at 125 °C, with an LTPD of 1.3.
Specifications subject to change without notice.

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 3.3 V, –40°C ≤ $T_A$ ≤ +85°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| TEMPERATURE COEFFICIENT[1, 2] | | | | | | |
| E Grade | $TCV_O$/°C | $I_{OUT}$ = 0 mA | | 2 | 5 | ppm/°C |
| F Grade | | | | 5 | 10 | ppm/°C |
| G Grade[3] | | | | 10 | 25 | ppm/°C |
| LINE REGULATION[4] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{IN}$ | 3.0 V ≤ $V_S$ ≤ 15 V, $I_{OUT}$ = 0 mA | | 5 | 10 | ppm/V |
| F and G Grades | | | | 10 | 20 | ppm/V |
| LOAD REGULATION[4] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S$ = 5.0 V, 0 mA ≤ $I_{OUT}$ ≤ 25 C | | 5 | 15 | ppm/mA |
| F and G Grades | | | | 10 | 20 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S$ = 3.15 V, $I_{LOAD}$ = 2 mA | | | 0.95 | V |
| | | $V_S$ = 3.3 V, $I_{LOAD}$ = 10 mA | | | 1.25 | V |
| | | $V_S$ = 3.6 V, $I_{LOAD}$ = 25 mA | | | 1.55 | V |
| $\overline{\text{SLEEP}}$ PIN | | | | | | |
| Logic High Input Voltage | $V_H$ | | 2.4 | | | V |
| Logic High Input Current | $I_H$ | | | | –8 | µA |
| Logic Low Input Voltage | $V_L$ | | | | 0.8 | V |
| Logic Low Input Current | $I_L$ | | | | –8 | µA |
| SUPPLY CURRENT | | No Load | | | 45 | µA |
| Sleep Mode | | No Load | | | 15 | µA |

NOTES
[1]For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2]$TCV_O$ is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/ °C.
$$TCV_O = (V_{MAX} - V_{MIN})/ V_O(T_{MAX} - T_{MIN}).$$
[3]Guaranteed by characterization.
[4]Line and load regulation specifications include the effect of self-heating.
Specifications subject to change without notice.

# REF191–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 3.3 V, –40°C ≤ $T_A$ ≤ +125°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| TEMPERATURE COEFFICIENT[1, 2] | | | | | | |
| E Grade | $TCV_O$/°C | $I_{OUT}$ = 0 mA | | 2 | | ppm/°C |
| F Grade | | | | 5 | | ppm/°C |
| G Grade[3] | | | | 10 | | ppm/°C |
| LINE REGULATION[4] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{IN}$ | 3.0 V ≤ $V_S$ ≤ 15 V, $I_{OUT}$ = 0 mA | | 10 | | ppm/V |
| F and G Grades | | | | 20 | | ppm/V |
| LOAD REGULATION[4] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S$ = 5.0 V, 0 mA ≤ $I_{OUT}$ ≤ 20 mA | | 10 | | ppm/mA |
| F and G Grades | | | | 20 | | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S$ = 3.3 V, $I_{LOAD}$ = 10 mA | | | 1.25 | V |
| | | $V_S$ = 3.6 V, $I_{LOAD}$ = 20 mA | | | 1.55 | V |

NOTES

[1]For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.

[2]$TCV_O$ is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.

$$TCV_O = (V_{MAX} - V_{MIN})/V_O(T_{MAX} - T_{MIN}).$$

[3]Guaranteed by characterization.

[4]Line and load regulation specifications include the effect of self-heating.

Specifications subject to change without notice.

# REF192–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 3.3 V, $T_A$ = 25°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INITIAL ACCURACY[1] | | | | | | |
| E Grade | $V_O$ | $I_{OUT}$ = 0 mA | 2.498 | 2.500 | 2.502 | V |
| F Grade | | | 2.495 | | 2.505 | V |
| G Grade | | | 2.490 | | 2.510 | V |
| LINE REGULATION[2] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{IN}$ | 3.0 V ≤ $V_S$ ≤ 15 V, $I_{OUT}$ = 0 mA | | 2 | 4 | ppm/V |
| F and G Grades | | | | 4 | 8 | ppm/V |
| LOAD REGULATION[2] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S$ = 5.0 V, 0 mA ≤ $I_{OUT}$ ≤ 30 mA | | 4 | 10 | ppm/mA |
| F and G Grades | | | | 6 | 15 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S$ = 3.5 V, $I_{LOAD}$ = 10 mA | | | 1.00 | V |
| | | $V_S$ = 3.9 V, $I_{LOAD}$ = 30 mA | | | 1.40 | V |
| LONG-TERM STABILITY[3] | $DV_O$ | 1,000 Hours @ 125°C | | 1.2 | | mV |
| NOISE VOLTAGE | $e_N$ | 0.1 Hz to 10 Hz | | 25 | | µV p-p |

NOTES
[1]Initial accuracy includes temperature hysteresis effect.
[2]Line and load regulation specifications include the effect of self-heating.
[3]Long-term drift is guaranteed by 1,000 hours life test performed on three independent wafer lots at 125°C, with an LTPD of 1.3.
Specifications subject to change without notice.

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 3.3 V, $T_A$ = –40°C ≤ $T_A$ ≤ +85°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| TEMPERATURE COEFFICIENT[1, 2] | | | | | | |
| E Grade | $TCV_O$/°C | $I_{OUT}$ = 0 mA | | 2 | 5 | ppm/°C |
| F Grade | | | | 5 | 10 | ppm/°C |
| G Grade[3] | | | | 10 | 25 | ppm/°C |
| LINE REGULATION[4] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{IN}$ | 3.0 V ≤ $V_S$ ≤ 15 V, $I_{OUT}$ = 0 mA | | 5 | 10 | ppm/V |
| F and G Grades | | | | 10 | 20 | ppm/V |
| LOAD REGULATION[4] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S$ = 5.0 V, 0 mA ≤ $I_{OUT}$ ≤ 25 mA | | 5 | 15 | ppm/mA |
| F and G Grades | | | | 10 | 20 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S$ = 3.5 V, $I_{LOAD}$ = 10 mA | | | 1.00 | V |
| | | $V_S$ = 4.0 V, $I_{LOAD}$ = 25 mA | | | 1.50 | V |
| $\overline{\text{SLEEP}}$ PIN | | | | | | |
| Logic High Input Voltage | $V_H$ | | 2.4 | | | V |
| Logic High Input Current | $I_H$ | | | | –8 | µA |
| Logic Low Input Voltage | $V_L$ | | | | 0.8 | V |
| Logic Low Input Current | $I_L$ | | | | –8 | µA |
| SUPPLY CURRENT | | No Load | | | 45 | µA |
| Sleep Mode | | No Load | | | 15 | µA |

NOTES
[1]For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2]$TCV_O$ is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.

$$TCV_O = (V_{MAX} - V_{MIN})/ V_O(T_{MAX} - T_{MIN}).$$

[3]Guaranteed by characterization.
[4]Line and load regulation specifications include the effect of self-heating.
Specifications subject to change without notice.

# REF192–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 3.3 V, –40°C ≤ $T_A$ ≤ +125°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| TEMPERATURE COEFFICIENT[1, 2] | | | | | | |
| E Grade | $TCV_O$/°C | $I_{OUT}$ = 0 mA | | 2 | | ppm/°C |
| F Grade | | | | 5 | | ppm/°C |
| G Grade[3] | | | | 10 | | ppm/°C |
| LINE REGULATION[4] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{IN}$ | 3.0 V ≤ $V_S$ ≤ 15 V, $I_{OUT}$ = 0 mA | | 10 | | ppm/V |
| F and G Grades | | | | 20 | | ppm/V |
| LOAD REGULATION[4] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S$ = 5.0 V, 0 mA ≤ $I_{OUT}$ ≤ 20 mA | | 10 | | ppm/mA |
| F and G Grades | | | | 20 | | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S$ = 3.5 V, $I_{LOAD}$ = 10 mA | | | 1.00 | V |
| | | $V_S$ = 4.0 V, $I_{LOAD}$ = 20 mA | | | 1.50 | V |

NOTES
[1]For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2]$TCV_O$ is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.

$$TCV_O = (V_{MAX} - V_{MIN})/ V_O(T_{MAX} - T_{MIN}).$$

[3]Guaranteed by characterization.
[4]Line and load regulation specifications include the effect of self-heating.
Specifications subject to change without notice.

# REF193–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 3.3 V, $T_A$ = 25°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INITIAL ACCURACY[1] | | | | | | |
| G Grade | $V_O$ | $I_{OUT}$ = 0 mA | 2.990 | 3.0 | 3.010 | V |
| LINE REGULATION[2] | | | | | | |
| G Grades | $\Delta V_O/\Delta V_{IN}$ | 3.3 V, ≤ $V_S$ ≤ 15 V, $I_{OUT}$ = 0 mA | | 4 | 8 | ppm/V |
| LOAD REGULATION[2] | | | | | | |
| G Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S$ = 5.0 V, 0 mA ≤ $I_{OUT}$ ≤ 30 mA | | 6 | 15 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S$ = 3.8 V, $I_{LOAD}$ = 10 mA | | | 0.80 | V |
| | | $V_S$ = 4.0 V, $I_{LOAD}$ = 30 mA | | | 1.00 | V |
| LONG-TERM STABILITY[3] | $DV_O$ | 1,000 Hours @ 125°C | | 1.2 | | mV |
| NOISE VOLTAGE | $e_N$ | 0.1 Hz to 10 Hz | | 30 | | µV p-p |

NOTES
[1]Initial accuracy includes temperature hysteresis effect.
[2]Line and load regulation specifications include the effect of self-heating.
[3]Long-term drift is guaranteed by 1,000 hours life test performed on three independent wafer lots at 125°C, with an LTPD of 1.3.
Specifications subject to change without notice.

# REF193–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 3.3 V, $T_A$ = –40°C ≤ $T_A$ ≤ +85°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| TEMPERATURE COEFFICIENT[1, 2] | | | | | | |
| G Grade[3] | $TCV_O$/°C | $I_{OUT}$ = 0 mA | | 10 | 25 | ppm/°C |
| LINE REGULATION[4] | | | | | | |
| G Grade | $\Delta V_O/\Delta V_{IN}$ | 3.3 V ≤ $V_S$ ≤ 15 V, $I_{OUT}$ = 0 mA | | 10 | 20 | ppm/V |
| LOAD REGULATION[4] | | | | | | |
| G Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S$ = 5.0 V, 0 mA ≤ $I_{OUT}$ ≤ 25 mA | | 10 | 20 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S$ = 3.8 V, $I_{LOAD}$ = 10 mA | | | 0.80 | V |
| | | $V_S$ = 4.1 V, $I_{LOAD}$ = 30 mA | | | 1.10 | V |
| $\overline{\text{SLEEP}}$ PIN | | | | | | |
| Logic High Input Voltage | $V_H$ | | 2.4 | | | V |
| Logic High Input Current | $I_H$ | | | | –8 | µA |
| Logic Low Input Voltage | $V_L$ | | | | 0.8 | V |
| Logic Low Input Current | $I_L$ | | | | –8 | µA |
| SUPPLY CURRENT | | No Load | | | 45 | µA |
| Sleep Mode | | No Load | | | 15 | µA |

NOTES
[1]For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2]$TCV_O$ is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/ °C.

$$TCV_O = (V_{MAX} - V_{MIN})/ V_O(T_{MAX} - T_{MIN}).$$

[3]Guaranteed by characterization.
[4]Line and load regulation specifications include the effect of self-heating.
Specifications subject to change without notice.

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 3.3 V, –40°C ≤ $T_A$ ≤ +125°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| TEMPERATURE COEFFICIENT[1, 2] | | | | | | |
| G Grade[3] | $TCV_O$/°C | $I_{OUT}$ = 0 mA | | 10 | | ppm/°C |
| LINE REGULATION[4] | | | | | | |
| G Grade | $\Delta V_O/\Delta V_{IN}$ | 3.3 V ≤ $V_S$ ≤ 15 V, $I_{OUT}$ = 0 mA | | 20 | | ppm/V |
| LOAD REGULATION[4] | | | | | | |
| G Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S$ = 5.0 V, 0 mA ≤ $I_{OUT}$ ≤ 20 mA | | 10 | | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S$ = 3.8 V, $I_{LOAD}$ = 10 mA | | | 0.80 | V |
| | | $V_S$ = 4.1 V, $I_{LOAD}$ = 20 mA | | | 1.10 | V |

NOTES
[1]For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2]$TCV_O$ is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/ °C.

$$TCV_O = (V_{MAX} - V_{MIN})/ V_O(T_{MAX} - T_{MIN}).$$

[3]Guaranteed by characterization.
[4]Line and load regulation specifications include the effect of self-heating.
Specifications subject to change without notice.

# REF194–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 5.0 V, $T_A$ = 25°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INITIAL ACCURACY[1] | | | | | | |
| E Grade | $V_O$ | $I_{OUT}$ = 0 mA | 4.498 | 4.5 | 4.502 | V |
| F Grade | | | 4.495 | | 4.505 | V |
| G Grade | | | 4.490 | | 4.510 | V |
| LINE REGULATION[2] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{IN}$ | 4.75 V ≤ $V_S$ ≤ 15 V, $I_{OUT}$ = 0 mA | | 2 | 4 | ppm/V |
| F and G Grades | | | | 4 | 8 | ppm/V |
| LOAD REGULATION[2] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S$ = 5.8 V, 0 mA ≤ $I_{OUT}$ ≤ 30 mA | | 2 | 4 | ppm/mA |
| F and G Grades | | | | 4 | 8 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S$ = 5.00 V, $I_{LOAD}$ = 10 mA | | | 0.50 | V |
| | | $V_S$ = 5.8 V, $I_{LOAD}$ = 30 mA | | | 1.30 | V |
| LONG-TERM STABILITY[3] | $DV_O$ | 1,000 Hours @ 125°C | | 2 | | mV |
| NOISE VOLTAGE | $e_N$ | 0.1 Hz to 10 Hz | | 45 | | µV p-p |

NOTES
[1]Initial accuracy includes temperature hysteresis effect.
[2]Line and load regulation specifications include the effect of self-heating.
[3]Long-term drift is guaranteed by 1,000 hours life test performed on three independent wafer lots at 125°C, with an LTPD of 1.3.
Specifications subject to change without notice.

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 5.0 V, $T_A$ = –40°C ≤ $T_A$ ≤ +85°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| TEMPERATURE COEFFICIENT[1, 2] | | | | | | |
| E Grade | $TCV_O$/°C | $I_{OUT}$ = 0 mA | | 2 | 5 | ppm/°C |
| F Grade | | | | 5 | 10 | ppm/°C |
| G Grade[3] | | | | 10 | 25 | ppm/°C |
| LINE REGULATION[4] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{IN}$ | 4.75 V ≤ $V_S$ ≤ 15 V, $I_{OUT}$ = 0 mA | | 5 | 10 | ppm/V |
| F and G Grades | | | | 10 | 20 | ppm/V |
| LOAD REGULATION[4] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S$ = 5.80 V, 0 mA ≤ $I_{OUT}$ ≤ 25 mA | | 5 | 15 | ppm/mA |
| F and G Grades | | | | 10 | 20 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S$ = 5.00 V, $I_{LOAD}$ = 10 mA | | | 0.5 | V |
| | | $V_S$ = 5.80 V, $I_{LOAD}$ = 25 mA | | | 1.30 | V |
| $\overline{\text{SLEEP}}$ PIN | | | | | | |
| Logic High Input Voltage | $V_H$ | | 2.4 | | | V |
| Logic High Input Current | $I_H$ | | | | –8 | µA |
| Logic Low Input Voltage | $V_L$ | | | | 0.8 | V |
| Logic Low Input Current | $I_L$ | | | | –8 | µA |
| SUPPLY CURRENT | | No Load | | | 45 | µA |
| Sleep Mode | | No Load | | | 15 | µA |

NOTES
[1]For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2]$TCV_O$ is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.

$$TCV_O = (V_{MAX} - V_{MIN})/ V_O(T_{MAX} - T_{MIN}).$$

[3]Guaranteed by characterization.
[4]Line and load regulation specifications include the effect of self-heating.
Specifications subject to change without notice.

# REF194–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 5.0 V, –40°C ≤ $T_A$ ≤ +125°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| TEMPERATURE COEFFICIENT[1, 2] | | | | | | |
| E Grade | $TCV_O$/°C | $I_{OUT}$ = 0 mA | | 2 | | ppm/°C |
| F Grade | | | | 5 | | ppm/°C |
| G Grade[3] | | | | 10 | | ppm/°C |
| LINE REGULATION[4] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{IN}$ | 4.75 V ≤ $V_S$ ≤ 15 V, $I_{OUT}$ = 0 mA | | 5 | | ppm/V |
| F and G Grades | | | | 10 | | ppm/V |
| LOAD REGULATION[4] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S$ = 5.80 V, mA 0 ≤ $I_{OUT}$ ≤ 20 mA | | 5 | | ppm/mA |
| F and G Grades | | | | 10 | | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S$ = 5.10 V, $I_{LOAD}$ = 10 mA | | | 0.60 | V |
| | | $V_S$ = 5.95 V, $I_{LOAD}$ = 20 mA | | | 1.45 | V |

NOTES

[1]For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.

[2]$TCV_O$ is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/ °C.

$$TCV_O = (V_{MAX} - V_{MIN})/ V_O(T_{MAX} - T_{MIN}).$$

[3]Guaranteed by characterization.

[4]Line and load regulation specifications include the effect of self-heating.

Specifications subject to change without notice.

# REF195–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 5.10 V, $T_A$ = 25°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INITIAL ACCURACY[1] | | | | | | |
| E Grade | $V_O$ | $I_{OUT}$ = 0 mA | 4.998 | 5.0 | 5.002 | V |
| F Grade | | | 4.995 | | 5.005 | V |
| G Grade | | | 4.990 | | 5.010 | V |
| LINE REGULATION[2] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{IN}$ | 5.10 V ≤ $V_S$ ≤ 15 V, $I_{OUT}$ = 0 mA | | 2 | 4 | ppm/V |
| F and G Grades | | | | 4 | 8 | ppm/V |
| LOAD REGULATION[2] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S$ = 6.30 V, 0 mA ≤ $I_{OUT}$ ≤ 30 mA | | 2 | 4 | ppm/mA |
| F and G Grades | | | | 4 | 8 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S$ = 5.50 V, $I_{LOAD}$ = 10 mA | | | 0.50 | V |
| | | $V_S$ = 6.30 V, $I_{LOAD}$ = 30 mA | | | 1.30 | V |
| LONG-TERM STABILITY[3] | $DV_O$ | 1,000 Hours @ 125°C | | 1.2 | | mV |
| NOISE VOLTAGE | $e_N$ | 0.1 Hz to 10 Hz | | 50 | | µV p-p |

NOTES
[1]Initial accuracy includes temperature hysteresis effect.
[2]Line and load regulation specifications include the effect of self-heating.
[3]Long-term drift is guaranteed by 1,000 hours life test performed on three independent wafer lots at 125°C, with an LTPD of 1.3.
Specifications subject to change without notice.

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 5.15 V, $T_A$ = –40°C ≤ $T_A$ ≤ +85°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| TEMPERATURE COEFFICIENT[1, 2] | | | | | | |
| E Grade | $TCV_O$/°C | $I_{OUT}$ = 0 mA | | 2 | 5 | ppm/°C |
| F Grade | | | | 5 | 10 | ppm/°C |
| G Grade[3] | | | | 10 | 25 | ppm/°C |
| LINE REGULATION[4] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{IN}$ | 5.15 V ≤ $V_S$ ≤ 15 V, $I_{OUT}$ = 0 mA | | 5 | 10 | ppm/V |
| F and G Grades | | | | 10 | 20 | ppm/V |
| LOAD REGULATION[4] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S$ = 6.30 V, 0 mA ≤ $I_{OUT}$ ≤ 25 mA | | 5 | 10 | ppm/mA |
| F and G Grades | | | | 10 | 20 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S$ = 5.50 V, $I_{LOAD}$ = 10 mA | | | 0.50 | V |
| | | $V_S$ = 6.30 V, $I_{LOAD}$ = 25 mA | | | 1.30 | V |
| $\overline{\text{SLEEP}}$ PIN | | | | | | |
| Logic High Input Voltage | $V_H$ | | 2.4 | | | V |
| Logic High Input Current | $I_H$ | | | | –8 | µA |
| Logic Low Input Voltage | $V_L$ | | | | 0.8 | V |
| Logic Low Input Current | $I_L$ | | | | –8 | µA |
| SUPPLY CURRENT | | No Load | | | 45 | µA |
| Sleep Mode | | No Load | | | 15 | µA |

NOTES
[1]For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2]$TCV_O$ is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.

$$TCV_O = (V_{MAX} - V_{MIN})/\ V_O(T_{MAX} - T_{MIN}).$$

[3]Guaranteed by characterization.
[4]Line and load regulation specifications include the effect of self-heating.
Specifications subject to change without notice.

# REF195–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 5.20 V, –40°C ≤ $T_A$ ≤ +125°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| TEMPERATURE COEFFICIENT[1, 2] | | | | | | |
| E Grade | $TCV_O$/°C | $I_{OUT}$ = 0 mA | | 2 | | ppm/°C |
| F Grade | | | | 5 | | ppm/°C |
| G Grade[3] | | | | 10 | | ppm/°C |
| LINE REGULATION[4] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{IN}$ | 5.20 V ≤ $V_S$ ≤ 15 V, $I_{OUT}$ = 0 mA | | 5 | | ppm/V |
| F and G Grades | | | | 10 | | ppm/V |
| LOAD REGULATION[4] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S$ = 6.45 V, 0 mA ≤ $I_{OUT}$ ≤ 20 mA | | 5 | | ppm/mA |
| F and G Grades | | | | 10 | | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S$ = 5.60 V, $I_{LOAD}$ = 10 mA | | | 0.60 | V |
| | | $V_S$ = 6.45 V, $I_{LOAD}$ = 20 mA | | | 1.45 | V |

NOTES
[1]For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2]$TCV_O$ is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/ °C.
$$TCV_O = (V_{MAX} - V_{MIN})/ V_O(T_{MAX} - T_{MIN}).$$
[3]Guaranteed by characterization.
[4]Line and load regulation specifications include the effect of self-heating.
Specifications subject to change without notice.

# REF196–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 3.5 V, $T_A$ = 25°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INITIAL ACCURACY[1] | | | | | | |
| G Grade | $V_O$ | $I_{OUT}$ = 0 mA | 3.290 | 3.3 | 3.310 | V |
| LINE REGULATION[2] | | | | | | |
| G Grades | $\Delta V_O/\Delta V_{IN}$ | 3.50 V ≤ $V_S$ ≤ 15 V, $I_{OUT}$ = 0 mA | | 4 | 8 | ppm/V |
| LOAD REGULATION[2] | | | | | | |
| G Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S$ = 5.0 V, 0 mA ≤ $I_{OUT}$ ≤ 30 mA | | 6 | 15 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S$ = 4.1 V, $I_{LOAD}$ = 10 mA | | | 0.80 | V |
| | | $V_S$ = 4.3 V, $I_{LOAD}$ = 30 mA | | | 1.00 | V |
| LONG-TERM STABILITY[3] | $DV_O$ | 1,000 Hours @ 125°C | | 1.2 | | mV |
| NOISE VOLTAGE | $e_N$ | 0.1 Hz to 10 Hz | | 33 | | µV p-p |

NOTES
[1]Initial accuracy includes temperature hysteresis effect.
[2]Line and load regulation specifications include the effect of self-heating.
[3]Long-term drift is guaranteed by 1,000 hours life test performed on three independent wafer lots at 125 °C, with an LTPD of 1.3.
Specifications subject to change without notice.

# REF196–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 3.5 V, $T_A$ = –40°C ≤ $T_A$ ≤ +85°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| TEMPERATURE COEFFICIENT[1, 2] | | | | | | |
| G Grade[3] | $TCV_O$/°C | $I_{OUT}$ = 0 mA | | 10 | 25 | ppm/°C |
| LINE REGULATION[4] | | | | | | |
| G Grade | $\Delta V_O/\Delta V_{IN}$ | 3.5 V ≤ $V_S$ ≤ 15 V, $I_{OUT}$ = 0 mA | | 10 | 20 | ppm/V |
| LOAD REGULATION[4] | | | | | | |
| G Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S$ = 5.0 V, 0 mA ≤ $I_{OUT}$ ≤ 25 mA | | 10 | 20 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S$ = 4.1 V, $I_{LOAD}$ = 10 mA | | | 0.80 | V |
| | | $V_S$ = 4.3 V, $I_{LOAD}$ = 25 mA | | | 1.00 | V |
| $\overline{\text{SLEEP}}$ PIN | | | | | | |
| Logic High Input Voltage | $V_H$ | | 2.4 | | | V |
| Logic High Input Current | $I_H$ | | | | –8 | µA |
| Logic Low Input Voltage | $V_L$ | | | | 0.8 | V |
| Logic Low Input Current | $I_L$ | | | | –8 | µA |
| SUPPLY CURRENT | | No Load | | | 45 | µA |
| Sleep Mode | | No Load | | | 15 | µA |

NOTES
[1]For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2]$TCV_O$ is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.

$$TCV_O = (V_{MAX} - V_{MIN})/V_O(T_{MAX} - T_{MIN}).$$

[3]Guaranteed by characterization.
[4]Line and load regulation specifications include the effect of self-heating.
Specifications subject to change without notice.

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 3.50 V, –40°C ≤ $T_A$ ≤ +125°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| TEMPERATURE COEFFICIENT[1, 2] | | | | | | |
| G Grade[3] | $TCV_O$/°C | $I_{OUT}$ = 0 mA | | 10 | | ppm/°C |
| LINE REGULATION[4] | | | | | | |
| G Grade | $\Delta V_O/\Delta V_{IN}$ | 3.50 V ≤ $V_S$ ≤ 15 V, $I_{OUT}$ = 0 mA | | 20 | | ppm/V |
| LOAD REGULATION[4] | | | | | | |
| G Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S$ = 5.0 V, 0 mA ≤ $I_{OUT}$ ≤ 20 mA | | 20 | | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S$ = 4.1 V, $I_{LOAD}$ = 10 mA | | | 0.80 | V |
| | | $V_S$ = 4.4 V, $I_{LOAD}$ = 20 mA | | | 1.10 | V |

NOTES
[1]For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.
[2]$TCV_O$ is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.

$$TCV_O = (V_{MAX} - V_{MIN})/V_O(T_{MAX} - T_{MIN}).$$

[3]Guaranteed by characterization.
[4]Line and load regulation specifications include the effect of self-heating.
Specifications subject to change without notice.

# REF198–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 5.0 V, $T_A$ = 25°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INITIAL ACCURACY[1] | | | | | | |
| E Grade | $V_O$ | $I_{OUT}$ = 0 mA | 4.094 | 4.096 | 4.098 | V |
| F Grade | | | 4.091 | | 4.101 | V |
| G Grade | | | 4.086 | | 4.106 | V |
| LINE REGULATION[2] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{IN}$ | 4.5 V ≤ $V_S$ ≤ 15 V, $I_{OUT}$ = 0 mA | | 2 | 4 | ppm/V |
| F and G Grades | | | | 4 | 8 | ppm/V |
| LOAD REGULATION[2] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S$ = 5.4 V, 0 mA ≤ $I_{OUT}$ ≤ 30 mA | | 2 | 4 | ppm/mA |
| F and G Grades | | | | 4 | 8 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S$ = 4.6 V, $I_{LOAD}$ = 10 mA | | | 0.50 | V |
| | | $V_S$ = 5.4 V, $I_{LOAD}$ = 30 mA | | | 1.30 | V |
| LONG-TERM STABILITY[3] | $DV_O$ | 1,000 Hours @ 125°C | | 1.2 | | mV |
| NOISE VOLTAGE | $e_N$ | 0.1 Hz to 10 Hz | | 40 | | μV p-p |

NOTES
[1]Initial accuracy includes temperature hysteresis effect.
[2]Line and load regulation specifications include the effect of self-heating.
[3]Long-term drift is guaranteed by 1,000 hours life test performed on three independent wafer lots at 125°C, with an LTPD of 1.3.
Specifications subject to change without notice.

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 5.0 V, –40°C ≤ $T_A$ ≤ +85°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| TEMPERATURE COEFFICIENT[1, 2] | | | | | | |
| E Grade | $TCV_O$/°C | $I_{OUT}$ = 0 mA | | 2 | 5 | ppm/°C |
| F Grade | | | | 5 | 10 | ppm/°C |
| G Grade[3] | | | | 10 | 25 | ppm/°C |
| LINE REGULATION[4] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{IN}$ | 4.5 V ≤ $V_S$ ≤ 15 V, $I_{OUT}$ = 0 mA | | 5 | 10 | ppm/V |
| F and G Grades | | | | 10 | 20 | ppm/V |
| LOAD REGULATION[4] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S$ = 5.4 V, 0 mA ≤ $I_{OUT}$ ≤ 25 mA | | 5 | 10 | ppm/mA |
| F and G Grades | | | | 10 | 20 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S$ = 4.6 V, $I_{LOAD}$ = 10 mA | | | 0.50 | V |
| | | $V_S$ = 5.4 V, $I_{LOAD}$ = 25 mA | | | 1.30 | V |
| $\overline{\text{SLEEP}}$ PIN | | | | | | |
| Logic High Input Voltage | $V_H$ | | 2.4 | | | V |
| Logic High Input Current | $I_H$ | | | | –8 | μA |
| Logic Low Input Voltage | $V_L$ | | | | 0.8 | V |
| Logic Low Input Current | $I_L$ | | | | –8 | μA |
| SUPPLY CURRENT | | No Load | | | 45 | μA |
| Sleep Mode | | No Load | | | 15 | μA |

NOTES
[1]For proper operation, a 1 μF capacitor is required between the output pin and the GND pin of the device.
[2]$TCV_O$ is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.

$$TCV_O = (V_{MAX} - V_{MIN})/ V_O(T_{MAX} - T_{MIN}).$$

[3]Guaranteed by characterization.
[4]Line and load regulation specifications include the effect of self-heating.
Specifications subject to change without notice.

# REF198–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 5.0 V, –40°C ≤ $T_A$ ≤ +125°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| TEMPERATURE COEFFICIENT[1, 2] | | | | | | |
| E Grade | $TCV_O$/°C | $I_{OUT}$ = 0 mA | | 2 | | ppm/°C |
| F Grade | | | | 5 | | ppm/°C |
| G Grade[3] | | | | 10 | | ppm/°C |
| LINE REGULATION[4] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{IN}$ | 4.5 V ≤ $V_S$ ≤ 15 V, $I_{OUT}$ = 0 mA | | 5 | | ppm/V |
| F and G Grades | | | | 10 | | ppm/V |
| LOAD REGULATION[4] | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S$ = 5.6 V, 0 mA ≤ $I_{OUT}$ ≤ 20 mA | | 5 | | ppm/mA |
| F and G Grades | | | | 10 | | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S$ = 4.7 V, $I_{LOAD}$ = 10 mA | | | 0.60 | V |
| | | $V_S$ = 5.6 V, $I_{LOAD}$ = 20 mA | | | 1.50 | V |

NOTES

[1]For proper operation, a 1 µF capacitor is required between the output pin and the GND pin of the device.

[2]$TCV_O$ is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.

$$TCV_O = (V_{MAX} - V_{MIN})/ V_O(T_{MAX} - T_{MIN}).$$

[3]Guaranteed by characterization.

[4]Line and load regulation specifications include the effect of self-heating.

Specifications subject to change without notice.

## WAFER TEST LIMITS (@ $I_{LOAD}$ = 0 mA, $T_A$ = 25°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Limit | Unit |
|---|---|---|---|---|
| INITIAL ACCURACY | | | | |
| REF191 | $V_O$ | | 2.043/2.053 | V |
| REF192 | | | 2.495/2.505 | V |
| REF193 | | | 2.990/3.010 | V |
| REF194 | | | 4.495/4.505 | V |
| REF195 | | | 4.995/5.005 | V |
| REF196 | | | 3.290/3.310 | V |
| REF198 | | | 4.091/4.101 | V |
| LINE REGULATION | $\Delta V_O/\Delta V_{IN}$ | ($V_O$ + 0.5 V) < $V_{IN}$ < 15 V, $I_{OUT}$ = 0 mA | 15 | ppm/V |
| LOAD REGULATION | $\Delta V_O/\Delta I_{LOAD}$ | 0 mA < $I_{LOAD}$ < 30 mA, $V_{IN}$ = ($V_O$ + 1.3 V) | 15 | ppm/mA |
| DROPOUT VOLTAGE | $V_O$ – V+ | $I_{LOAD}$ = 10 mA | 1.25 | V |
| | | $I_{LOAD}$ = 30 mA | 1.55 | V |
| $\overline{\text{SLEEP}}$ MODE INPUT | | | | |
| Logic Input High | $V_{IH}$ | | 2.4 | V |
| Logic Input Low | $V_{IL}$ | | 0.8 | V |
| SUPPLY CURRENT | $V_{IN}$ = 15 V | No Load | 45 | µA |
| Sleep Mode | | No Load | 15 | µA |

For proper operation, a 1 µF capacitor is required between the output pins and the GND pin of the REF19x. Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

**ABSOLUTE MAXIMUM RATINGS**[1, 2]

Supply Voltage . . . . . –0.3 V, +18 V
Output to GND . . . . . –0.3 V, $V_S$ + 0.3 V
Output to GND Short-Circuit Duration . . . . . Indefinite
Storage Temperature Range
P, S Package . . . . . –65°C to +150°C
Operating Temperature Range
REF19x . . . . . –40°C to +85°C
Junction Temperature Range
P, S Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

| Package Type | $\theta_{JA}$[3] | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 8-Lead PDIP (P) | 103 | 43 | °C/W |
| 8-Lead SOIC (S) | 158 | 43 | °C/W |
| 8-Lead TSSOP (RU) | 240 | 43 | °C/W |

NOTES
[1] Absolute maximum rating applies to both DICE and packaged parts, unless otherwise noted.
[2] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[3] $\theta_{JA}$ is specified for worst-case conditions, i.e., $\theta_{JA}$ is specified for device in socket for PDIP, and $\theta_{JA}$ is specified for device soldered in circuit board for SOIC package.

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the REF19x features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

**ORDERING GUIDE**

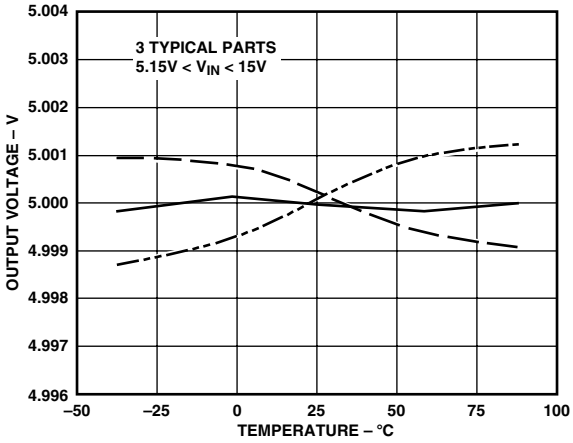
| Model | Temperature Range | Package Description | Package Option | Minimum Quantities/ Reel |
|---|---|---|---|---|
| REF191ES | –40°C to +85°C | 8-Lead SOIC | R-8 | |
| REF191ES-REEL | –40°C to +85°C | 8-Lead SOIC | R-8 | 2,500 |
| REF191GP | –40°C to +85°C | 8-Lead PDIP | N-8 | |
| REF191GS | –40°C to +85°C | 8-Lead SOIC | R-8 | |
| REF191GS-REEL7 | –40°C to +85°C | 8-Lead SOIC | R-8 | 1,000 |
| REF192ES | –40°C to +85°C | 8-Lead SOIC | R-8 | |
| REF192ES-REEL | –40°C to +85°C | 8-Lead SOIC | R-8 | 2,500 |
| REF192ES-REEL7 | –40°C to +85°C | 8-Lead SOIC | R-8 | 1,000 |
| REF192FS | –40°C to +85°C | 8-Lead SOIC | R-8 | |
| REF192FS-REEL | –40°C to +85°C | 8-Lead SOIC | R-8 | 2,500 |
| REF192FS-REEL7 | –40°C to +85°C | 8-Lead SOIC | R-8 | 1,000 |
| REF192FSZ-REEL7* | –40°C to +85°C | 8-Lead SOIC | R-8 | 1,000 |
| REF192GP | –40°C to +85°C | 8-Lead PDIP | N-8 | |
| REF192GRU | –40°C to +85°C | 8-Lead TSSOP | RU-8 | |
| REF192GRU-REEL7 | –40°C to +85°C | 8-Lead TSSOP | RU-8 | 1,000 |
| REF192GS | –40°C to +85°C | 8-Lead SOIC | R-8 | |
| REF192GS-REEL | –40°C to +85°C | 8-Lead SOIC | R-8 | 2,500 |
| REF192GS-REEL7 | –40°C to +85°C | 8-Lead SOIC | R-8 | 1,000 |
| REF192GSZ-REEL7* | –40°C to +85°C | 8-Lead SOIC | R-8 | 1,000 |

**ORDERING GUIDE (continued)**

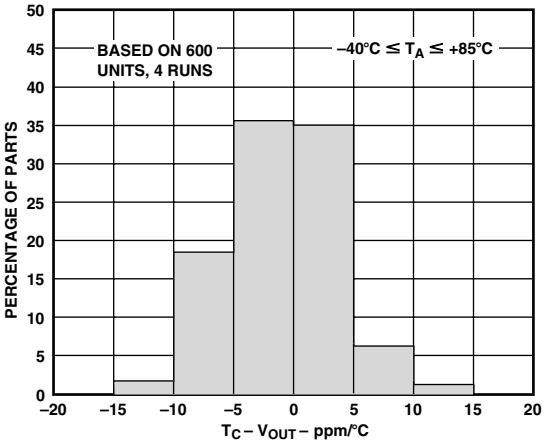
| Model | Temperature Range | Package Description | Package Option | Minimum Quantities/ Reel |
|---|---|---|---|---|
| REF193GS | –40°C to +85°C | 8-Lead SOIC | R-8 | |
| REF193GS-REEL | –40°C to +85°C | 8-Lead SOIC | R-8 | 2,500 |
| REF194ES | –40°C to +85°C | 8-Lead SOIC | R-8 | |
| REF194ES-REEL | –40°C to +85°C | 8-Lead SOIC | R-8 | 2,500 |
| REF194FS | –40°C to +85°C | 8-Lead SOIC | R-8 | |
| REF194GP | –40°C to +85°C | 8-Lead PDIP | N-8 | |
| REF194GS | –40°C to +85°C | 8-Lead SOIC | R-8 | |
| REF194GS-REEL | –40°C to +85°C | 8-Lead SOIC | R-8 | 2,500 |
| REF194GS-REEL7 | –40°C to +85°C | 8-Lead SOIC | R-8 | 1,000 |
| REF195ES | –40°C to +85°C | 8-Lead SOIC | R-8 | |
| REF195ES-REEL | –40°C to +85°C | 8-Lead SOIC | R-8 | 2,500 |
| REF195FS | –40°C to +85°C | 8-Lead SOIC | R-8 | |
| REF195FS-REEL | –40°C to +85°C | 8-Lead SOIC | R-8 | 2,500 |
| REF195GP | –40°C to +85°C | 8-Lead PDIP | N-8 | |
| REF195GRU | –40°C to +85°C | 8-Lead TSSOP | RU-8 | |
| REF195GRU-REEL7 | –40°C to +85°C | 8-Lead TSSOP | RU-8 | 1,000 |
| REF195GS | –40°C to +85°C | 8-Lead SOIC | R-8 | |
| REF195GS-REEL | –40°C to +85°C | 8-Lead SOIC | R-8 | 2,500 |
| REF195GS-REEL7 | –40°C to +85°C | 8-Lead SOIC | R-8 | 1,000 |
| REF195GSZ-REEL7* | –40°C to +85°C | 8-Lead SOIC | R-8 | 1,000 |
| REF196GRU-REEL7 | –40°C to +85°C | 8-Lead TSSOP | RU-8 | 1,000 |
| REF196GS | –40°C to +85°C | 8-Lead SOIC | R-8 | |
| REF196GS-REEL | –40°C to +85°C | 8-Lead SOIC | R-8 | 2,500 |
| REF196GSZ-REEL7* | –40°C to +85°C | 8-Lead SOIC | R-8 | 1,000 |
| REF198ES | –40°C to +85°C | 8-Lead SOIC | R-8 | |
| REF198ES-REEL | –40°C to +85°C | 8-Lead SOIC | R-8 | 2,500 |
| REF198FS | –40°C to +85°C | 8-Lead SOIC | R-8 | |
| REF198FS-REEL | –40°C to +85°C | 8-Lead SOIC | R-8 | 2,500 |
| REF198GP | –40°C to +85°C | 8-Lead PDIP | N-8 | |
| REF198GRU | –40°C to +85°C | 8-Lead TSSOP | RU-8 | |
| REF198GRU-REEL7 | –40°C to +85°C | 8-Lead TSSOP | RU-8 | 1,000 |
| REF198GS | –40°C to +85°C | 8-Lead SOIC | R-8 | |
| REF198GS-REEL | –40°C to +85°C | 8-Lead SOIC | R-8 | 2,500 |

*Z = Pb-free part.

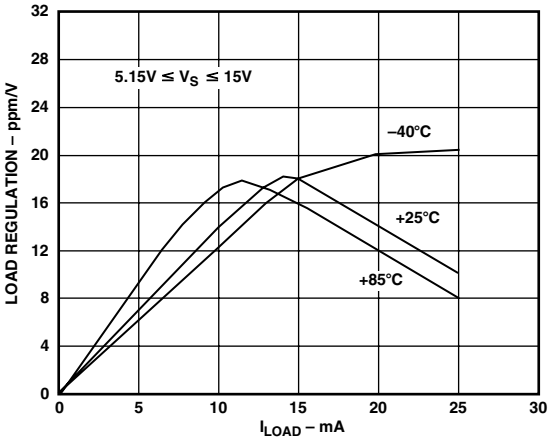
# REF19x Series–Typical Performance Characteristics



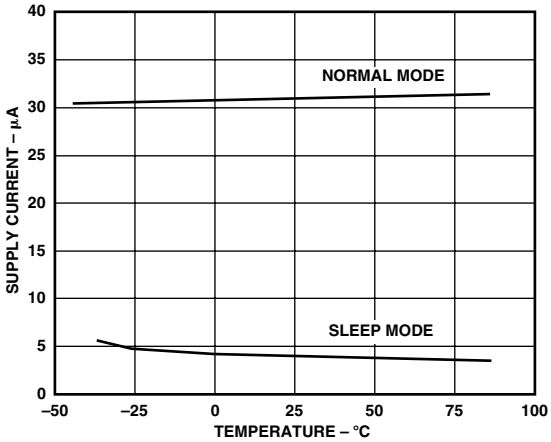

*TPC 1. REF195 Output Voltage vs. Temperature*



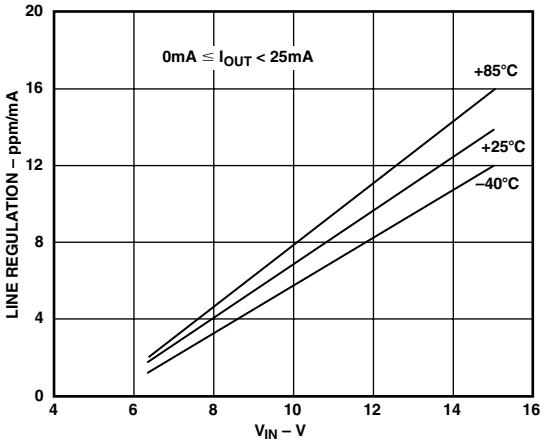

*TPC 4. $T_C$ – $V_{OUT}$ Distribution*



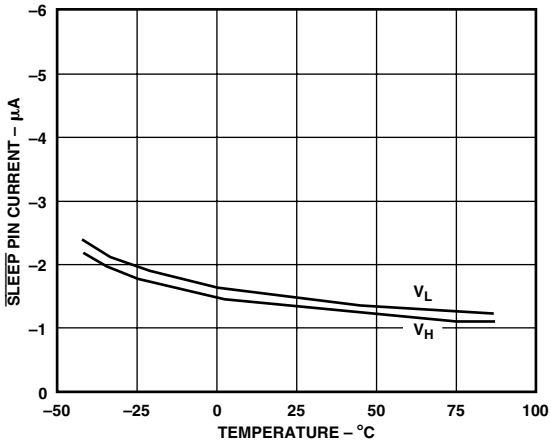

*TPC 2. REF195 Load Regulation vs. $I_{LOAD}$*



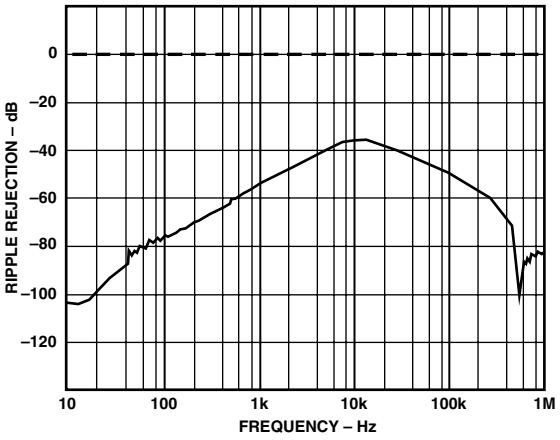

*TPC 5. Quiescent Current vs. Temperature*



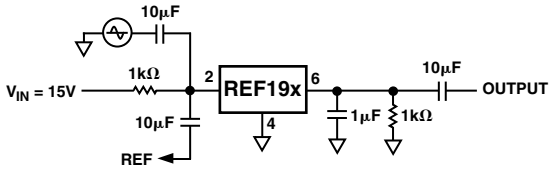

*TPC 3. REF195 Line Regulation vs. $V_{IN}$*



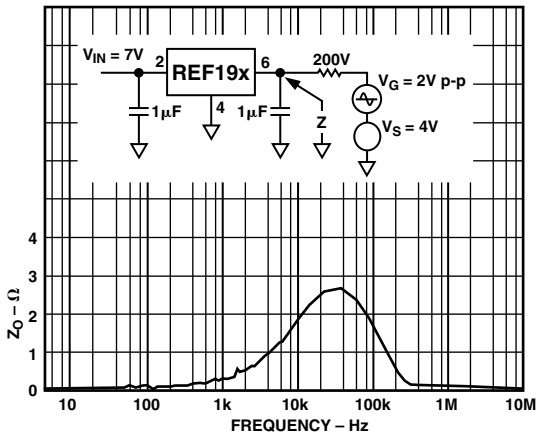

*TPC 6. $\overline{SLEEP}$ Pin Current vs. Temperature*



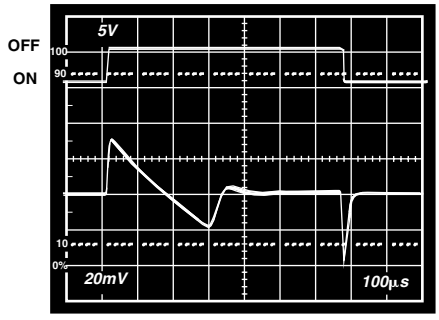

*TPC 7a. Ripple Rejection vs. Frequency*



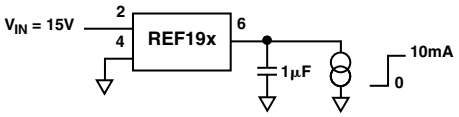

*TPC 7b. Ripple Rejection vs. Frequency Measurement Circuit*



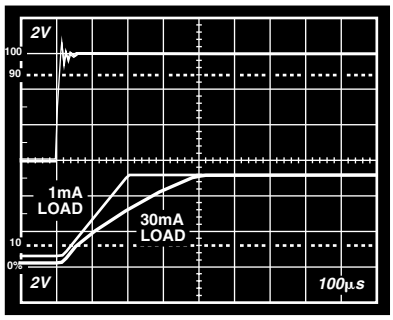

*TPC 8. Output Impedance vs. Frequency*



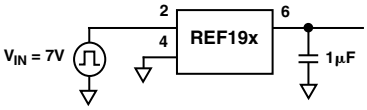

*TPC 9a. Load Transient Response*



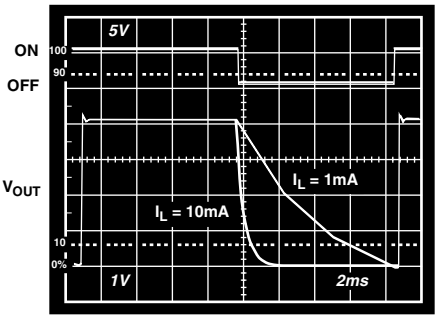

*TPC 9b. Load Transient Response Measurement Circuit*



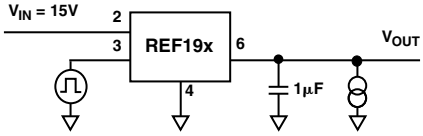

*TPC 10a. Power ON Response Time*



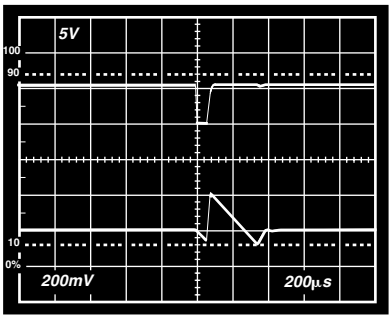

*TPC 10b. Power ON Response Time Measurement Circuit*



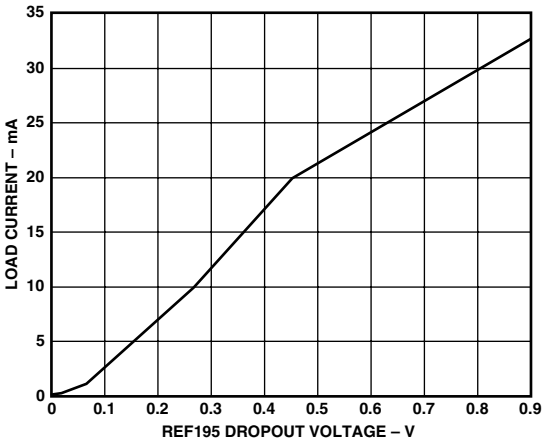

*TPC 11a. $\overline{SLEEP}$ Response Time*




*TPC 11b. $\overline{SLEEP}$ Response Time Measurement Circuit*




TPC 12. Line Transient Response




TPC 13. Load Current vs. Dropout Voltage

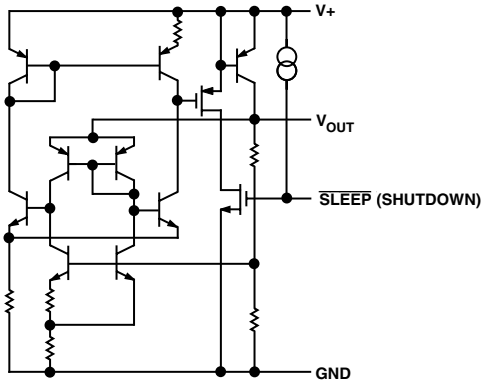



Figure 1. Simplified Schematic

## APPLICATIONS SECTION

### Output Short-Circuit Behavior

The REF19x family of devices is totally protected from damage due to accidental output shorts to GND or to V+. In the event of an accidental short-circuit condition, the reference device will shut down and limit its supply current to 40 mA.

### Device Power Dissipation Considerations

The REF19x family of references is capable of delivering load currents to 30 mA with an input voltage that ranges from 3.3 V to 15 V. When these devices are used in applications with large input voltages, care should be exercised to avoid exceeding these devices' maximum internal power dissipation. Exceeding the published specifications for maximum power dissipation or junction temperature could result in premature device failure. The following formula should be used to calculate a device's maximum junction temperature or dissipation:

$$P_D = \frac{T_J - T_A}{\theta_{JA}}$$

In this equation, $T_J$ and $T_A$ are the junction and ambient temperatures, respectively, $P_D$ is the device power dissipation, and $\theta_{JA}$ is the device package thermal resistance.

### Output Voltage Bypassing

For stable operation, low dropout voltage regulators and references generally require a bypass capacitor connected from their $V_{OUT}$ pins to their GND pins. Although the REF19x family of references is capable of stable operation with capacitive loads exceeding 100 µF, a 1 µF capacitor is sufficient to guarantee rated performance. The addition of a 0.1 µF ceramic capacitor in parallel with the bypass capacitor will improve load current transient performance. For best line voltage transient performance, it is recommended that the voltage inputs of these devices be bypassed with a 10 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor.

### Sleep Mode Operation

All REF19x devices include a sleep capability that is TTL/CMOS level compatible. Internally, a pull-up current source to $V_{IN}$ is connected at the $\overline{\text{SLEEP}}$ pin. This permits the $\overline{\text{SLEEP}}$ pin to be driven from an open collector/drain driver. A logic low or a 0 V condition on the $\overline{\text{SLEEP}}$ pin is required to turn off the output stage. During sleep, the output of the references becomes a high impedance state where its potential would then be determined by external circuitry. If the sleep feature is not used, it is recommended that the $\overline{\text{SLEEP}}$ pin be connected to $V_{IN}$ (Pin 2).

### Basic Voltage Reference Connections

The circuit in Figure 2 illustrates the basic configuration for the REF19x family of references. Note the 10 µF/0.1 µF bypass network on the input and the 1 µF/0.1 µF bypass network on the output. It is recommended that no connections be made to Pins 1, 5, 7, and 8. If the sleep feature is not required, Pin 3 should be connected to $V_{IN}$.

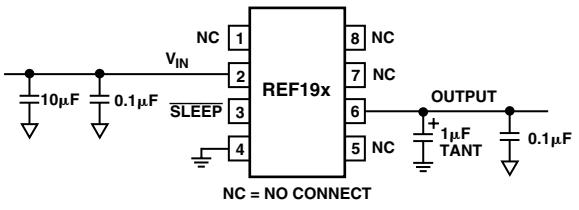



Figure 2. Basic Voltage Reference Configuration

**Membrane Switch Controlled Power Supply**

With output load currents in the tens of mA, the REF19x family of references can operate as a low dropout power supply in hand-held instrument applications. In the circuit shown in Figure 3, a membrane ON/OFF switch is used to control the operation of the reference. During an initial power-on condition, the $\overline{\text{SLEEP}}$ pin is held to GND by the 10 kΩ resistor. Recall that this condition disables (read: three-state) the REF19x output. When the membrane ON switch is pressed, the $\overline{\text{SLEEP}}$ pin is momentarily pulled to $V_{IN}$, enabling the REF19x output. At this point, current through the 10 kΩ is reduced and the internal current source connected to the $\overline{\text{SLEEP}}$ pin takes control. Pin 3 assumes and remains at the same potential as $V_{IN}$. When the membrane OFF switch is pressed, the $\overline{\text{SLEEP}}$ pin is momentarily connected to GND, which once again disables the REF19x output.

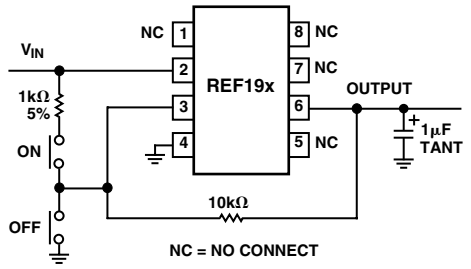



*Figure 3. Membrane Switch Controlled Power Supply*

**Current-Boosted References with Current Limiting**

While the 30 mA rated output current of the REF19x series is higher than typical of other reference ICs, it can be boosted to higher levels if desired with the addition of a simple external PNP transistor, as shown in Figure 4. Full-time current limiting is used for protection of the pass transistor against shorts.

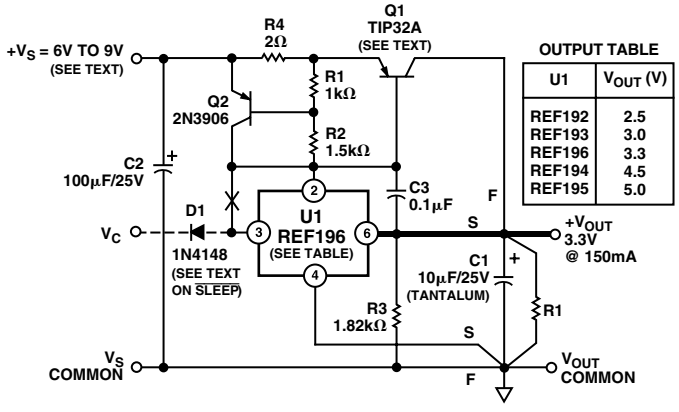



*Figure 4. A Boosted 3.3 V Reference with Current Limiting*

In this circuit, the power supply current of reference U1 flowing through R1 to R2 develops a base drive for Q1, whose collector provides the bulk of the output current. With a typical gain of 100 in Q1 for 100 mA to 200 mA loads, U1 is never required to furnish more than a few mA, so this factor minimizes temperature related drift. Short-circuit protection is provided by Q2, which clamps drive to Q1 at about 300 mA of load current with values as shown. With this separation of control and power functions, dc stability is optimum, allowing best advantage use of premium grade REF19x devices for U1. Of course, load management should still be exercised. A short, heavy, low DCR (dc resistance) conductor should be used from U1 to 6 to the $V_{OUT}$ sense point S, where the collector of Q1 connects to the load, point F.

Because of the current limiting configuration, the dropout voltage circuit is raised about 1.1 V over that of the REF19x devices, due to the $V_{BE}$ of Q1 and the drop across current sense resistor R4. However, overall dropout is typically still low enough to allow operation of a 5 V to 3.3 V regulator/reference using the REF196 for U1 as noted, with a $V_S$ as low as 4.5 V and a load current of 150 mA.

The requirement for a heat sink on Q1 depends on the maximum input voltage and short-circuit current. With $V_S$ = 5 V and a 300 mA current limit, the worst-case dissipation of Q1 is 1.5 W, less than the TO-220 package 2 W limit. However, if smaller TO-39 or TO-5 packaged devices, such as the 2N4033, are used, the current limit should be reduced to keep maximum dissipation below the package rating. This is accomplished by simply raising R4.

A tantalum output capacitor is used at C1 for its low ESR (equivalent series resistance), and the higher value is required for stability. Capacitor C2 provides input bypassing and can be an ordinary electrolytic.

Shutdown control of the booster stage is shown as an option, and when used, some cautions are needed. Because of the additional active devices in the $V_S$ line to U1, direct drive to Pin 3 does not work as with an unbuffered REF19x device. To enable shutdown control, the connection to U1 to U2 is broken at the X, and diode D1 then allows a CMOS control source $V_C$ to drive U1 to 3 for ON/OFF operation. Startup from shutdown is not as clean under heavy load as it is in basic REF19x series and can require several milliseconds under load. Nevertheless, it is still effective and can fully control 150 mA loads. When shutdown control is used, heavy capacitive loads should be minimized.

**A Negative Precision Reference without Precision Resistors**

In many current-output CMOS DAC applications where the output signal voltage must be of the same polarity as the reference voltage, it is often required to reconfigure a current-switching DAC into a voltage-switching DAC through the use of a 1.25 V reference, an op amp, and a pair of resistors. Using a current-switching DAC directly requires an additional operational amplifier at the output to reinvert the signal. A negative voltage reference is then desirable because an additional operational amplifier is not required for either reinversion (current-switching mode) or amplification (voltage-switching mode) of the DAC output voltage. In general, any positive voltage reference can be converted into a negative voltage reference through the use of an operational amplifier and a pair of matched resistors in an inverting configuration. The disadvantage to that approach is that the largest single source of error in the circuit is the relative matching of the resistors used.

The circuit illustrated in Figure 5 avoids the need for tightly matched resistors by using an active integrator circuit. In this circuit, the output of the voltage reference provides the input drive for the integrator. The integrator, to maintain circuit equilibrium, adjusts its output to establish the proper relationship between the reference's $V_{OUT}$ and GND. Thus, any desired negative output voltage can be chosen by simply substituting for the appropriate reference IC. The sleep feature is maintained in the circuit with the simple addition of a PNP transistor and a 10 kΩ resistor. One caveat with this approach should be mentioned: although rail-to-rail output amplifiers work best in the application, these operational amplifiers require a finite amount (mV) of headroom when required to provide any load current. The choice for the circuit's negative supply should take this issue into account.

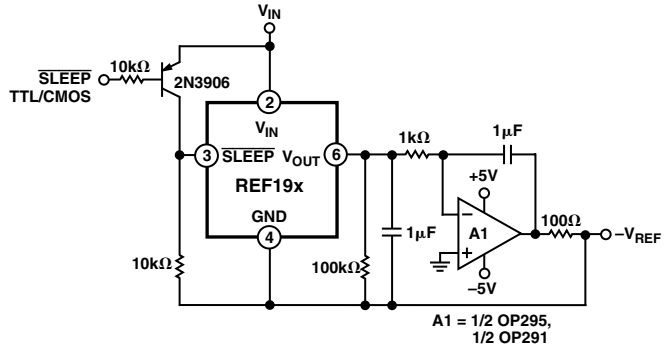



*Figure 5. A Negative Precision Voltage Reference Uses No Precision Resistors*

**Stacking Reference ICs for Arbitrary Outputs**

Some applications may require two reference voltage sources that are a combined sum of standard outputs. The circuit in Figure 6 shows how this stacked output reference can be implemented.

OUTPUT TABLE

| U1/U2 | $V_{OUT1}$ (V) | $V_{OUT2}$ (V) |
|---|---|---|
| REF192/REF192 | 2.5 | 5.0 |
| REF192/REF194 | 2.5 | 7.0 |
| REF192/REF195 | 2.5 | 7.5 |

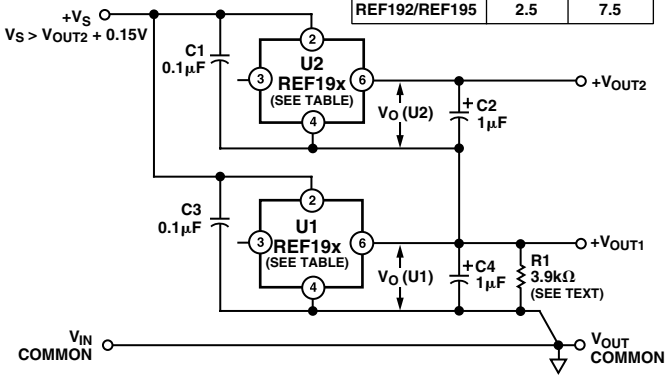



*Figure 6. Stacking Voltage References with the REF19x*

Two reference ICs are used, fed from a common unregulated input, $V_S$. The outputs of the individual ICs are simply connected in series as shown, which provides two output voltages, $V_{OUT1}$ and $V_{OUT2}$. $V_{OUT1}$ is the terminal voltage of U1, while $V_{OUT2}$ is the sum of this voltage and the terminal voltage of U2. U1 and U2 are simply chosen for the two voltages that supply the required outputs (see Table I). If, for example, both U1 and U2 are REF192s, the two outputs are 2.5 V and 5.0 V.

While this concept is simple, some cautions are needed. Since the lower reference circuit must sink a small bias current from U2 (50 μA to 100 μA), plus the base current from the series PNP output transistor in U2, either the external load of U1 or R1 must provide a path for this current. If the U1 minimum load is not well defined, Resistor R1 should be used, set to a value that will conservatively pass 600 μA of current with the applicable $V_{OUT1}$ across it. Note that the two U1 and U2 reference circuits are locally treated as macrocells, each having its own bypasses at input and output for best stability. Both U1 and U2 in this circuit can source dc currents up to their full rating. The minimum input voltage, $V_S$, is determined by the sum of the outputs, $V_{OUT2}$, plus the dropout voltage of U2.

A related variation on stacking two 3-terminal references is shown in Figure 6, where U1, a REF192, is stacked with a 2-terminal reference diode such as the AD589. Like the 3-terminal stacked reference above, this circuit provides two outputs, $V_{OUT1}$ and $V_{OUT2}$, which are the individual terminal voltages of D1 and U1, respectively. Here this is 1.235 and 2.5, which provides a $V_{OUT2}$ of 3.735 V. When using 2-terminal reference diodes, such as D1, the rated minimum and maximum device currents must be observed and the maximum load current from $V_{OUT1}$ can be no greater than the current set up by R1 and $V_{O(U1)}$. In the case with $V_{O(U1)}$ equal to 2.5 V, R1 provides a 500 μA bias to D1, so the maximum load current available at $V_{OUT1}$ is 450 μA or less.

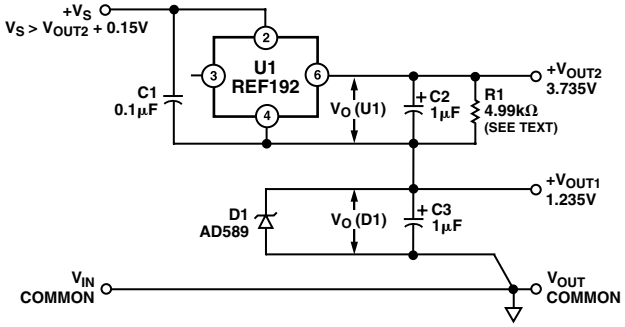



*Figure 7. Stacking Voltage References with the REF19x*

**A Precision Current Source**

Many times, in low power applications, the need arises for a precision current source that can operate on low supply voltages. As shown in Figure 8, any one of the devices in the REF19x family of references can be configured as a precision current source. The circuit configuration illustrated is a floating current source with a grounded load. The reference's output voltage is bootstrapped across $R_{SET}$, which sets the output current into the load. With this configuration, circuit precision is maintained for load currents in the range from the reference's supply current (typically, 30 μA) to approximately 30 mA. The low dropout voltage of these devices maximizes the current source's output voltage compliance without excess headroom.

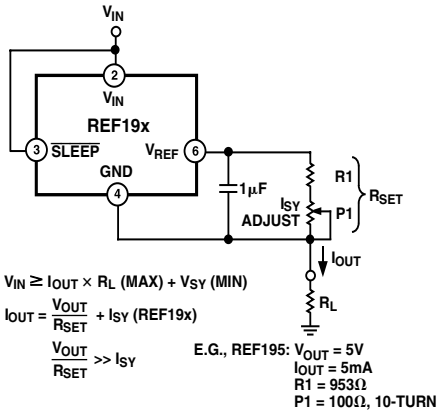



*Figure 8. A Low Dropout, Precision Current Source*

The circuit's governing equations are

$$V_{IN} = I_{OUT} \times R_L(Max) + V_{SY}(Min, REF19x)$$

$$I_{OUT} = \frac{V_{OUT}}{R_{SET}} + I_{SY}(REF19x)$$

$$\frac{V_{OUT}}{R_{SET}} \rangle\rangle I_{SY}(REF19x)$$

**Switched Output 5 V/3.3 V Reference**

Applications often require digital control of reference voltages, selecting between one stable voltage and a second. With the sleep feature inherent to the REF19x series, switched output reference configurations are easily implemented with relatively little additional hardware.

The circuit of Figure 9 illustrates the general technique, which takes advantage of the output "wire-OR" capability of the REF19x device family. When OFF, a REF19x device is effectively an open circuit at the output node with respect to the power supply. When ON, a REF19x device can source current up to its current rating, but sink only a few µA (essentially just the relatively low current of the internal output scaling divider). As a result, for two devices wired together at their common outputs, the output voltage is simply that of the ON device. The OFF state device will draw a small standby current of 15 µA (max), but otherwise will not interfere with operation of the ON device, which can operate to its full current rating. Note that the two devices in the circuit conveniently share both input and output capacitors, and with CMOS logic drive, it is power efficient.

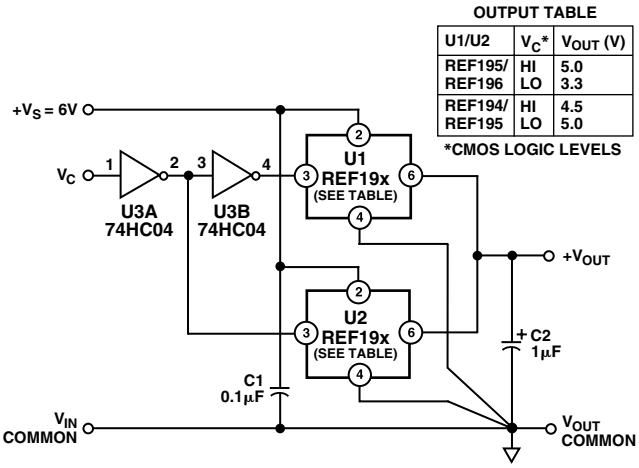



*Figure 9. Switched Output Reference*

Using dissimilar REF19x series devices with this configuration allows logic selection between the U1/U2 specified terminal voltages. For example, with U1 (a REF195) and U2 (a REF196), as noted in the table in Figure 9, changing the CMOS compatible $V_C$ logic control voltage from HI to LO selects between a nominal output of 5.000 V and 3.300 V and vice versa. Other REF19x family units can also be used for U1/U2, with similar operation in a logic sense, but with outputs as per the individual paired devices (see table again). Of course, the exact output voltage tolerance, drift, and overall quality of the reference voltage will be consistent with the grade of individual U1 and U2 devices.

Because of the nature of the wire-OR, there is one application caveat that should be understood about this circuit. Since U1 and U2 can only *source* current effectively, negative going output voltage changes, which require the *sinking* of current, will necessarily take longer than positive going changes. In practice, this means that the circuit is quite fast when undergoing a transition from 3.3 V to 5 V, but the transition from 5 V to 3.3 V will take longer. Exactly how much longer will be a function of the load resistance, $R_L$, seen at the output and the typical 1 µF value of C2. In general, a conservative transition time here will be on the order of several milliseconds for load resistances in the range of 100 Ω to 1 kΩ. Note that for highest accuracy at the new output voltage, several time constants should be allowed (>7.6 time constants for <1/2 LSB error @ 10 bits, for example).

**Kelvin Connections**

In many portable instrumentation applications where PC board cost and area go hand-in-hand, circuit interconnects are very often narrow. These narrow lines can cause large voltage drops if the voltage reference is required to provide load currents to various functions. In fact, a circuit's interconnects can exhibit a typical line resistance of 0.45 mΩ/square (1 oz. Cu, for example). In those applications where these devices are configured as low dropout voltage regulators, these wiring voltage drops can become a large source of error. To circumvent this problem, force and sense connections can be made to the reference through the use of an operational amplifier, as shown in Figure 10. This method provides a means by which the effects of wiring resistance voltage drops can be eliminated. Load currents flowing through wiring resistance produce an I-R error ($I_{LOAD} \times R_{WIRE}$) at the load. However, the Kelvin connection overcomes the problem by including the wiring resistance within the forcing loop of the op amp. Since the op amp senses the load voltage, op amp loop control forces the output to compensate for the wiring error and to produce the correct voltage at the load. Depending on the reference device chosen, operational amplifiers that can be used in this application are the OP295, the OP292, and the OP183.

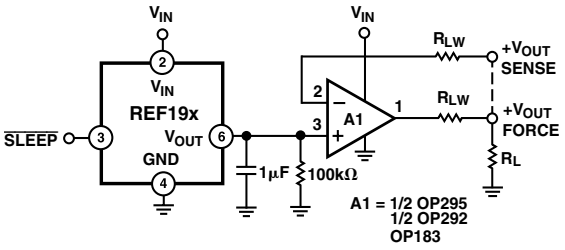



*Figure 10. A Low Dropout, Kelvin Connected Voltage Reference*

**A Fail-Safe 5 V Reference**

Some critical applications require a reference voltage to be maintained constant, even with a loss of primary power. The low standby power of the REF19x series and the switched output capability allow a fail-safe reference configuration to be implemented rather easily. This reference maintains a tight output voltage tolerance for either a primary power source (ac line derived) or a standby (battery derived) power source, automatically switching between the two as the power conditions change.

The circuit in Figure 11 illustrates the concept, which borrows from the switched output idea of Figure 8, again using the REF19x device family output wire-OR capability. In this case, since a constant 5 V reference voltage is desired for all conditions, two REF195 devices are used for U1 and U2, with their ON/OFF switching controlled by the presence or absence of the primary dc supply source, $V_S$. $V_{BAT}$ is a 6 V battery backup source that supplies power to the load only when $V_S$ fails. For normal ($V_S$ present) power conditions, $V_{BAT}$ sees only the 15 µA (max) standby current drain of U1 in its OFF state.

In operation, it is assumed that for all conditions either U1 or U2 is ON and a 5 V reference output is available. With this voltage constant, a scaled down version is applied to the comparator IC U3, providing a fixed 0.5 V input to the (–) input for all power conditions. The R1 to R2 divider provides a signal to the U3 (+) input proportional to $V_S$, which switches U3 and U1/U2 dependent upon the absolute level of $V_S$. Op amp U3 is configured here as a comparator with hysteresis, which provides for clean, noise-free output switching. This hysteresis is important to eliminate rapid switching at the threshold due to $V_S$ ripple. Further, the device chosen is the AD820, a rail-to-rail output device that provides HI and LO output states within a few mV of $V_S$ and ground for accurate thresholds and compatible drive for U2 for all $V_S$ conditions. R3 provides positive feedback for circuit hysteresis, changing the threshold at the (+) input as a function of U3's output.

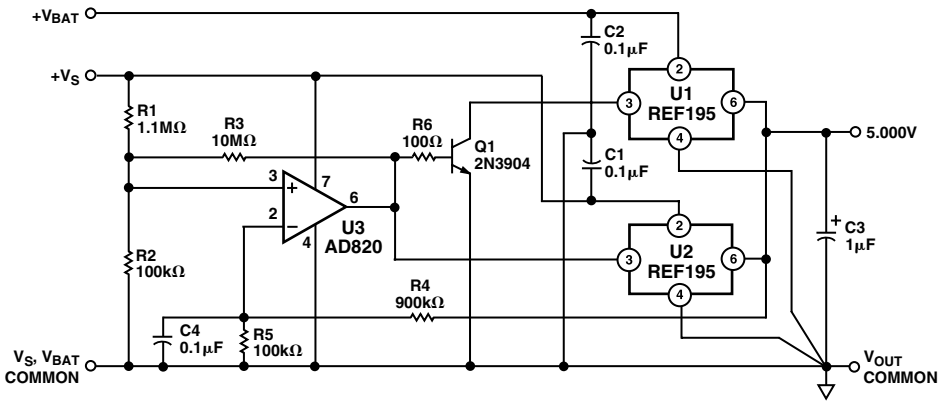



*Figure 11. A Fail-Safe 5 V Reference*

For $V_S$ levels lower than the LOWER threshold, U3's output is low, thus U2 and Q1 are OFF, while U1 is ON. For $V_S$ levels higher than the UPPER threshold, the situation reverses, with U1 OFF and both U2 and Q1 ON. In the interest of battery power conservation, all of the comparison switching circuitry is powered from $V_S$ and is arranged so that when $V_S$ fails, the default output comes from U1.

For the R1 to R3 values as shown, the LOWER/UPPER $V_S$ switching thresholds are approximately 5.5 V and 6 V, respectively. These can obviously be changed to suit other $V_S$ supplies, as can the REF19x devices used for U1 and U2, over a range of 2.5 V to 5 V of output. U3 can operate down to a $V_S$ of 3.3 V, which is generally compatible with all family devices.

**A Low Power, Strain Gage Circuit**

As shown in Figure 12, the REF19x family of references can be used in conjunction with low supply voltage operational amplifiers, such as the OP492 and the OP283, in a self-contained strain gage circuit. In this circuit, the REF195 was used as the core of this low power, strain gage circuit. Other references can be easily accommodated by changing circuit element values. The references play a dual role as the voltage regulator to provide the supply voltage requirements of the strain gage and the operational amplifiers as well as a precision voltage reference for the current source used to stimulate the bridge. A distinct feature of the circuit is that it can be remotely controlled ON or OFF by digital means via the $\overline{\text{SLEEP}}$ pin.

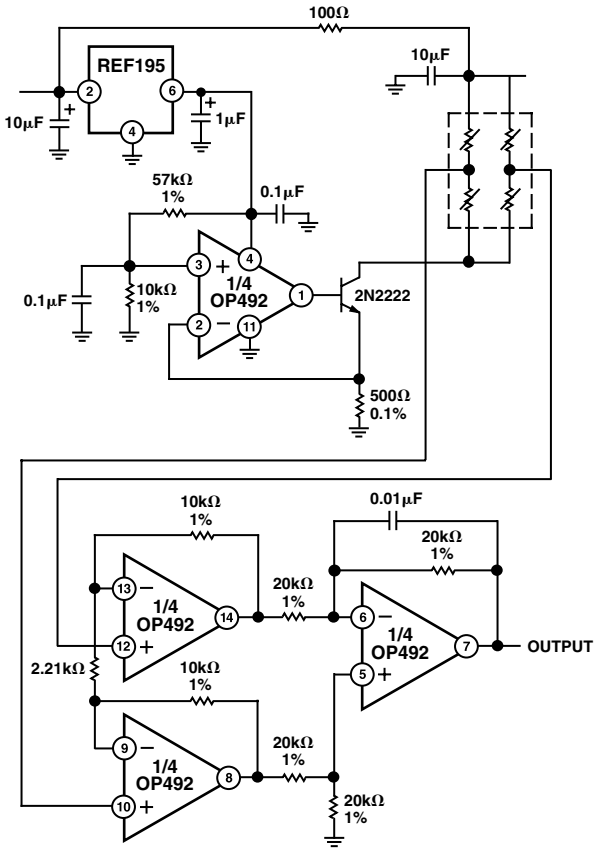
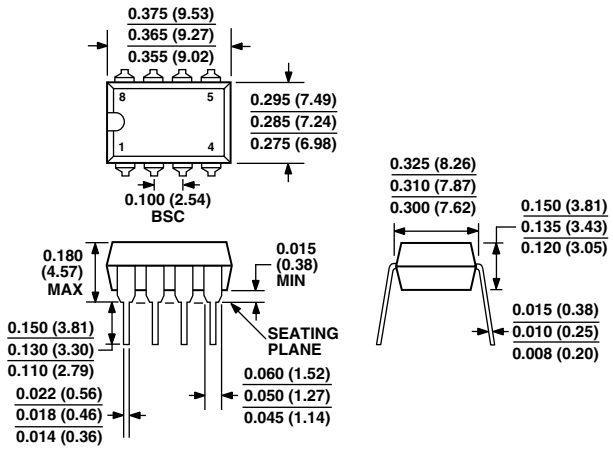



*Figure 12. A Low Power, Strain Gage Circuit*

## OUTLINE DIMENSIONS

### 8-Lead Plastic Dual In-Line Package [PDIP]
### (N-8)
### P-Suffix

Dimensions shown in inches and (millimeters)

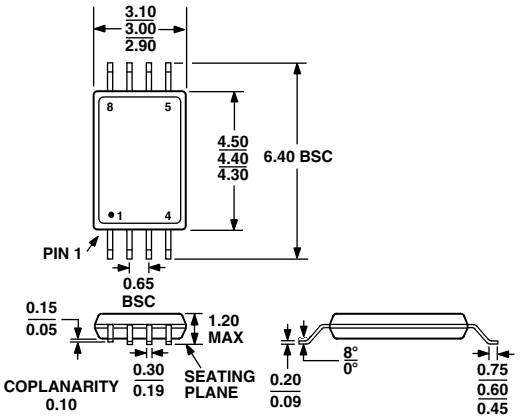



COMPLIANT TO JEDEC STANDARDS MO-095AA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

### 8-Lead Thin Shrink Small Outline Package [TSSOP]
### (RU-8)

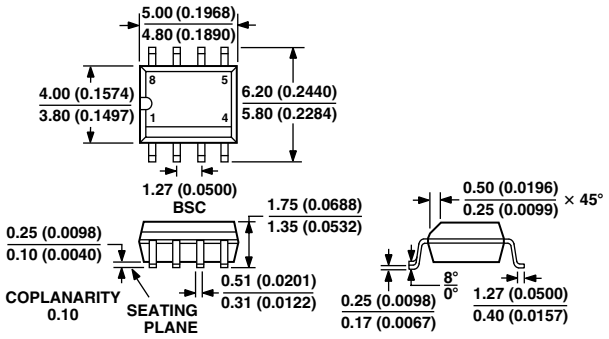
Dimensions shown in millimeters




COMPLIANT TO JEDEC STANDARDS MO-153AA

### 8-Lead Standard Small Outline Package [SOIC]
### Narrow Body
### (R-8)
### S-Suffix

Dimensions shown in millimeters and (inches)

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# Revision History


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| **3/04—Data Sheet changed from REV. E to REV. F.** | |
| Updated ABSOLUTE MAXIMUM RATINGS | 14 |
| Updated ORDERING GUIDE | 14 |
| Updated OUTLINE DIMENSIONS | 24 |
| **1/03—Data Sheet changed from REV. D to REV. E.** | |
| Changes to TPCs 2 and 3 | 15 |
| Changes to Output Short Circuit Behavior | 17 |
| Changes to Figure 1 | 17 |
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| Updated OUTLINE DIMENSIONS | 23 |

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