

PDSP16112/PDSP16112A

16 x 12 BIT COMPLEX MULTIPLIER

(SUPERSEDES MARCH 1987 EDITION)

The PDSP16112/PDSP16112A will multiply a complex (16 + 16) bit data word by a complex (12 + 12) bit coefficient word and produce a complex (17 + 17) bit rounded product. The input data format is two's complement. The device consists of four 16 x 12 multiplier sections based on Booth's '2 bits at a time' algorithm and is pipelined to achieve a 20MHz (PDSP16112A) or 10MHz (PDSP16112) throughput.

FEATURES

- 20MHz Complex Number (16 + 16) x (12 + 12) Multiplication
- Pipelined Architecture
- Power Dissipation only 500mW
- TTL Compatible Inputs
- Advanced 2 micron CMOS Process

APPLICATIONS

- Digital Filtering
- Fast Fourier Transforms
- Radar and Sonar Processing
- Instrumentation
- Automation
- Image Processing

ASSOCIATED PRODUCTS

- PDSP1601** Arithmetic Logic Unit
- PDSP1640** 40MHz Address Generator
- PDSP16318** Complex Accumulator
- PDSP16330** Pythagoras Processor

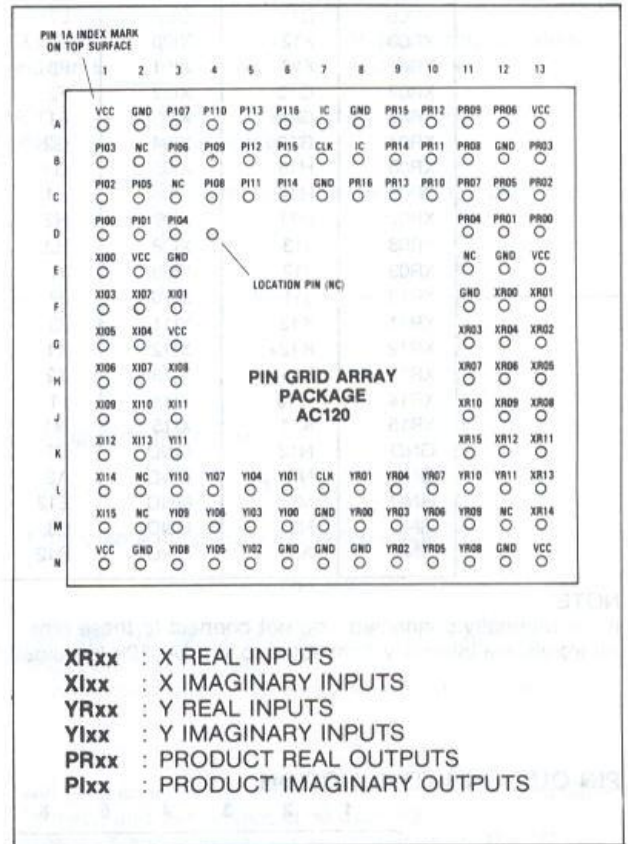


Fig.1 Pin connections - top view

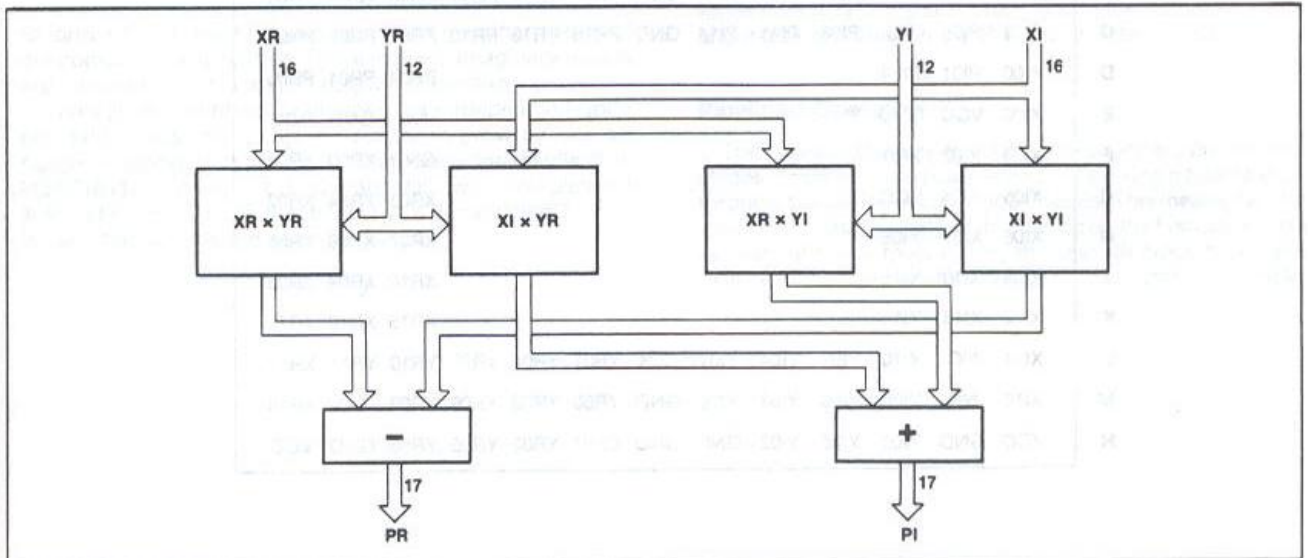


Fig.2 Multiplier block diagram

PIN OUT - FUNCTION TO PIN

Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.
PR00	D13	PR09	A11	PI00	D1	PI09	B4
PR01	D12	PR10	C10	PI01	D2	PI10	A4
PR02	C13	PR11	B10	PI02	C1	PI11	C5
PR03	B13	PR12	A10	PI03	B1	PI12	B5
PR04	D11	PR13	C9	PI04	D3	PI13	A5
PR05	C12	PR14	B9	PI05	C2	PI14	C6
PR06	A12	PR15	A9	PI06	B3	PI15	B6
PR07	C11	PR16	C8	PI07	A3	PI16	A6
PR08	B11	CLK	L7	PI08	C4	CLK	B7
XR00	F12	XI00	E1	YR00	M8	YI00	M6
XR01	F13	XI01	F3	YR01	L8	YI01	L6
XR02	G13	XI02	F2	YR02	N9	YI02	N5
XR03	G11	XI03	F1	YR03	M9	YI03	M5
XR04	G12	XI04	G2	YR04	L9	YI04	L5
XR05	H13	XI05	G1	YR05	N10	YI05	N4
XR06	H12	XI06	H1	YR06	M10	YI06	M4
XR07	H11	XI07	H2	YR07	L10	YI07	L4
XR08	J13	XI08	H3	YR08	N11	YI08	N3
XR09	J12	XI09	J1	YR09	M11	YI09	M3
XR10	J11	XI10	J2	YR10	L11	YI10	L3
XR11	K13	XI11	J3	YR11	L12	YI11	K3
XR12	K12	XI12	K1	NC	B2	NC	M12
XR13	L13	XI13	K2	NC	L2	NC	M2
XR14	M13	XI14	L1	VCC	A1	NC	E11
XR15	K11	XI15	M1	VCC	G3	NC	C3
GND	N12	GND	C7	VCC	E2	GND	N8
GND	N7	GND	A2	VCC	A13	GND	N6
GND	M7	GND	E12	VCC	E13	GND	F11
GND	N2	GND	E3	VCC	N1	IC	B8
GND	A8	GND	B12	VCC	N13	IC	A7

NOTE

IC = Internally connected - do not connect to these pins.
 All inputs are internally connected to Vcc by 10k (nominal) resistors.

PIN OUT - PIN TO FUNCTION

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	VCC	GND	PI07	PI10	PI13	PI16	IC	GND	PR15	PR12	PR09	PR06	VCC
B	PI03	NC	PI06	PI09	PI12	PI15	CLK	IC	PR14	PR11	PR08	GND	PR03
C	PI02	PI05	NC	PI08	PI11	PI14	GND	PR16	PR13	PR10	PR07	PR05	PR02
D	PI00	PI01	PI04								PR04	PR01	PR00
E	XI00	VCC	GND								NC	GND	VCC
F	XI03	XI02	XI01								GND	XR00	XR01
G	XI05	XI04	VCC								XR03	XR04	XR02
H	XI06	XI07	XI08								XR07	XR06	XR05
J	XI09	XI10	XI11								XR10	XR09	XR08
K	XI12	XI13	YI11								XR15	XR12	XR11
L	XI14	NC	YI10	YI07	YI04	YI01	CLK	YR01	YR04	YR07	YR10	YR11	XR13
M	XI15	NC	YI09	YI06	YI03	YI00	GND	YR00	YR03	YR06	YR09	NC	XR14
N	VCC	GND	YI08	YI05	YI02	GND	GND	GND	YR02	YR05	YR08	GND	VCC

PIN DESCRIPTION

XR00 - XR15	X Real Inputs : Two's Complement Format XR15 = MSB (Sign) XR00 = LSB For Fractional Arithmetic the Weighting of XR15 = 1 i.e. $-1 \leq XR < 1$	PR00 - PR16	P Real Outputs : Two's Complement Format PR16 = MSB (Sign) PR00 = LSB For Fractional Arithmetic the Weighting of PR16 = 2 i.e. $-2 \leq PR < 2$
XI00 - XI15	X Imag Inputs : Two's Complement Format XI15 = MSB (Sign) XI00 = LSB For Fractional Arithmetic the Weighting of XI15 = 1 i.e. $-1 \leq XI < 1$	PI00 - PI16	P Imag Outputs : Two's Complement Format PI16 = MSB (Sign) PI00 = LSB For Fractional Arithmetic the Weighting of PI16 = 2 i.e. $-2 \leq PI < 2$
YR00 - YR11	Y Real Inputs : Two's Complement Format YR11 = MSB (Sign) YR00 = LSB For Fractional Arithmetic the Weighting of YR11 = 1 i.e. $-1 \leq YR < 1$	CLK pin B7 and pin L7	Common Clock to all on chip registers, both pins must be connected
YI00 - YI11	Y Imag Inputs : Two's Complement Format YI11 = MSB (Sign) YI00 = LSB For Fractional Arithmetic the Weighting of YI11 = 1 i.e. $-1 \leq YI < 1$	VCC GND	All VCC and GND pins must be connected
		IC	Internally connected - do not use

FUNCTIONAL DESCRIPTION

The PDSP16112 Complex Multiplier contains four pipelined 16x12 Array Multipliers, a 17-bit adder and a 17-bit subtractor.

The multipliers accept data from the XR, XI, YR, and YI inputs and perform the four multiplies necessary to implement a Complex Multiply Operation,

$$(XR \times YR, XR \times YI, XI \times YR, XI \times YI).$$

The 28-bit results from these operations are rounded to the most significant 16-bits before being passed to the adder and subtractor. The subtractor calculates

$$(XR \times YR) - (XI \times YI)$$

to form a 17-bit result representing the real result of the complex multiplication. The adder calculates

$$(XR \times YI) + (XI \times YR)$$

to form a 17-bit result that represents the imaginary result of the complex multiplication. These real and imaginary results are passed to the PR and PI outputs respectively.

The add and subtract operations may, (depending upon the data), cause the multiplier results to grow by one bit hence requiring 17-bit outputs to represent the results. The PDSP16112 is designed to operate with two's complement arithmetic, hence if the Fractional two's complement format is used the outputs will lie in the range

$$-2 \leq P < 2$$

for inputs in the range

$$-1 \leq X \text{ or } Y < 1.$$

If the output magnitude lies in the range

$$-1 \leq P < 1,$$

then the 17th (MSB) bit of the outputs will duplicate the 16th (Sign) bit of the output.

In common with other Array multipliers, the operation

$$-1 \times -1$$

will yield an incorrect result for fractional two's complement formats, and hence should be avoided.

Both X and Y inputs are registered as are the PR and PI outputs. On the rising edge of CLK data present on the XR, XI, YR, and YI inputs is clocked into the input registers. At the same time a new result is clocked into the output registers and made available on the PR and PI output ports.

Pipelined Operation

The internal Multiply and Add operations are divided into stages by six internal pipeline registers giving a total latency through the device of eight clock cycles. This means that the result from data loaded into the device on the first clock cycle appears at the outputs during the seventh clock cycle, and may be loaded into another device on the eighth clock cycle.

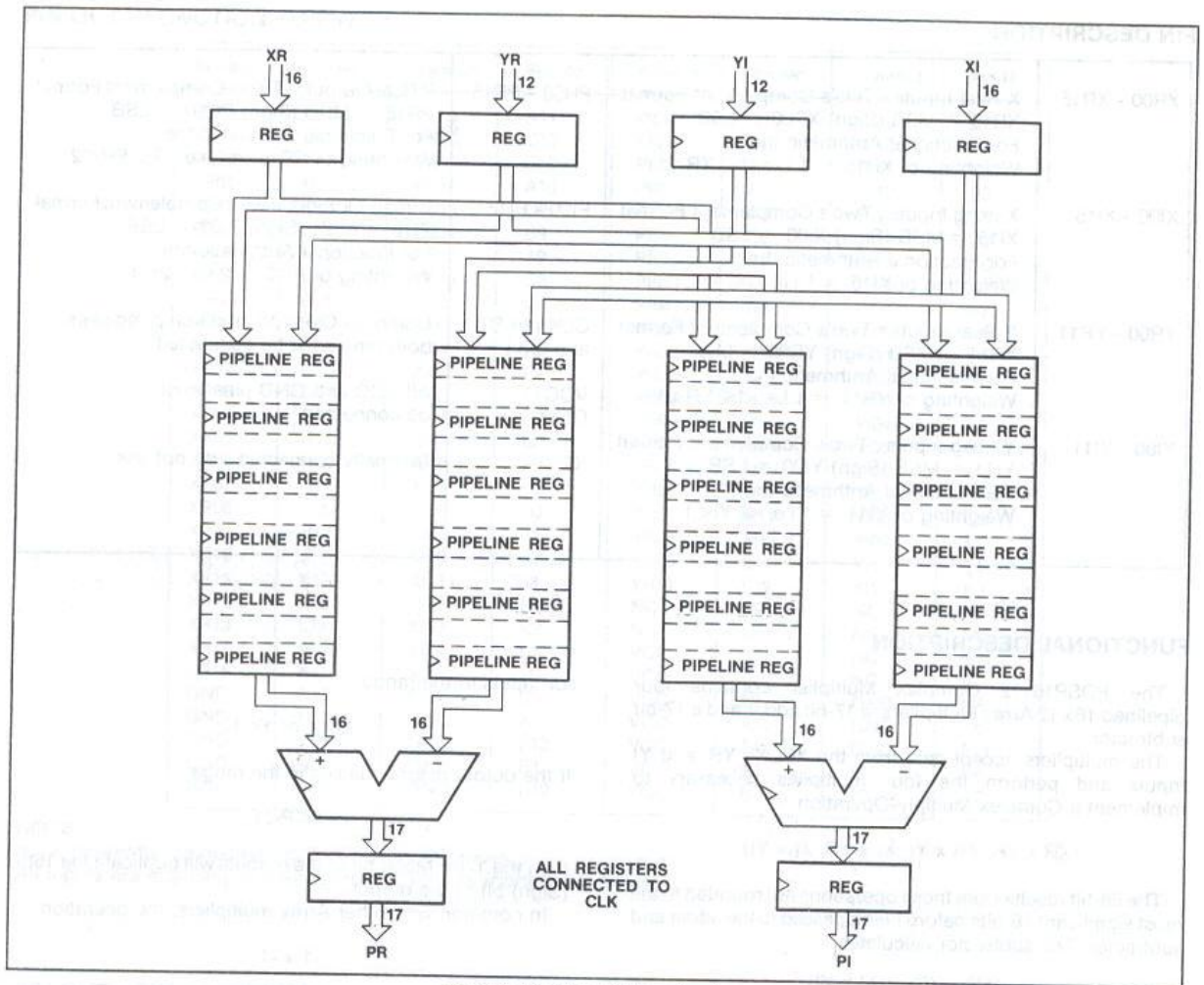


Fig.3 Pipelined multiplier structure

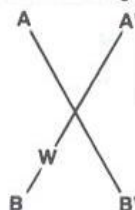
TYPICAL APPLICATION

The PDSP16112A may be configured as the main arithmetic element in a FFT Butterfly calculation. A single PDSP16112A together with two PDSP16318As will produce an arithmetic processor capable of executing a new Radix 2 DIT Butterfly every 50ns using 16-bit data and 12-bit coefficients. The PDSP16318A provides flags that monitor the magnitude of the output data, together with on chip shift circuits.

A single Butterfly processor of this type will allow the following FFT benchmarks.

- 1024 point complex radix 2 transform in 256μsecs
- 512 point complex radix 2 transform in 115μsecs
- 256 point complex radix 2 transform in 51μsecs

The arithmetic operation required to realise a radix 2 decimation in time algorithm is as follows.



$$A' = A + (B \times W)$$

$$B' = A - (B \times W)$$

Where A and B are the data inputs, A' and B' are the data outputs, and W is the coefficient. A,B,A',B' and W are all complex numbers i.e. they all have real and imaginary components. The Butterfly therefore requires one complex multiply and two complex adds to execute, which is equivalent to four real multiplies and six real adds.

Fig.4 illustrates the interconnection of the PDSP16112 with the two PDSP16318A Complex Accumulators. The PDSP16112 performs the complex multiply operation at the full 20MHz rate to provide the real and imaginary components of (B x W) to the two ALUs. The PDSP16318A is capable of 16-bit operations at 20MHz and has on chip register storage and Shifter. In every 20MHz cycle each PDSP16318A performs two arithmetic operations to calculate the real or imaginary parts of A + (B x W) and A - (B x W). One of the PDSP16318As calculates the real parts and the other calculates the imaginary parts.

For greater throughput one chip-set may be allocated to each column of the FFT. For example, a 1K complex FFT could be calculated by 10 chip-sets every 26μs.

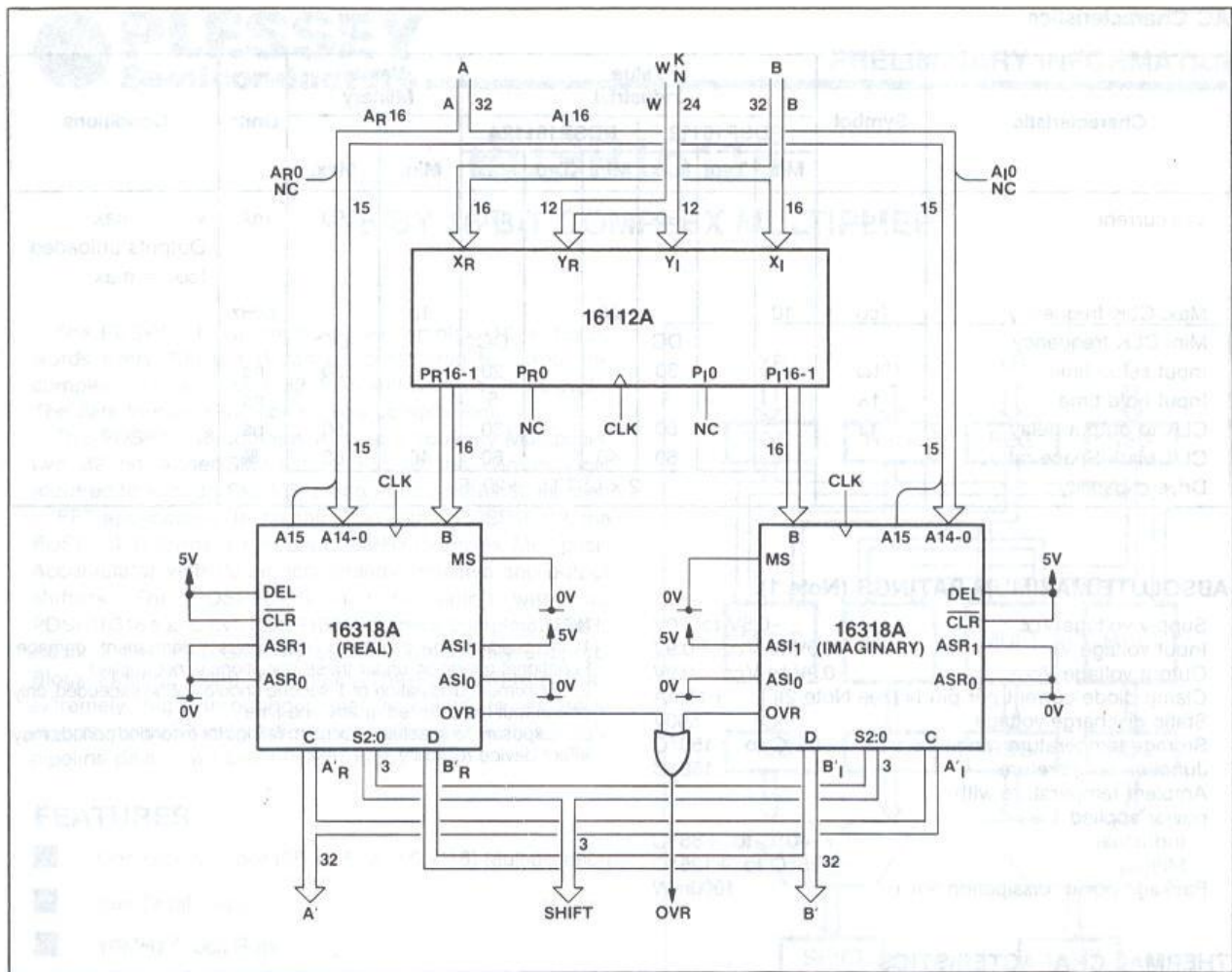


Fig.4 Radix 2 DIT butterfly processor

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

- T_{amb} (Industrial) = -40°C to +85°C, V_{cc} = 5.0V ± 10%, GND = 0V
- T_{amb} (Military) = -55°C to +125°C, V_{cc} = 5.0V ± 10%, GND = 0V

Static Characteristics

Characteristic	Symbol	Value						Units	Conditions
		PDSP16112			PDSP16112A				
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Output high voltage	V _{OH}	2.4			2.4			V	I _{OH} = 4mA
Output low voltage	V _{OL}			0.6			0.6	V	I _{OL} = 4mA
Input high voltage	V _{IH}	2.2			2.2			V	
Input low voltage	V _{IL}			0.8			0.8	V	
Input leakage current *	I _L	-1.0		+0.01	-1.0		+0.01	mA	GND ≤ V _{IN} ≤ V _{CC}
Output short circuit current	I _{OS}	15			20			mA	V _{CC} = max.
Input capacitance	C _I		10			10		pF	

* All inputs have a nominal 10K pull-up resistor to V_{cc}.

PDSP16112/A

AC Characteristics

Characteristic	Symbol	Value Industrial						Value Military		Units	Conditions	
		PDSP16112			PDSP16112A			Min.	Max.			
		Min.	Typ.	Max.	Min.	Typ.	Max.					
V _{CC} current	I _{CC}			90			170		90	mA	V _{CC} = max Outputs unloaded f _{CLK} = max	
Max. CLK frequency	f _{CLK}	10			20			10		MHz		
Min. CLK frequency				DC			DC		DC			
Input setup time	t _{su}			30			20		30	ns		
Input hold time	t _{ih}			5			5		5	ns		
CLK to output delay	t _d			50			30		50	ns		
CLK Mark/Space ratio		40		60	40		60	40	60	%		
Drive capability		2 x LSTTL +20pF										

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage V _{CC}	-0.5V to 7.0V
Input voltage V _{IN}	-0.9V to V _{CC} +0.9V
Output voltage V _{OUT}	-0.9V to V _{CC} +0.9V
Clamp diode current per pin I _k (see Note 2)	±18mA
Static discharge voltage	500V
Storage temperature range T _s	-65°C to +150°C
Junction temperature	150°C
Ambient temperature with power applied T _{amb}	
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Package power dissipation P _{tot}	1000mW

NOTES

- Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
- Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
- Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Package Type	θ _{JC} °C/W	θ _{JA} °C/W
AC	11	35

ORDERING INFORMATION

Industrial
PDSP16112 B0 AC
PDSP16112A B0 AC

Military
PDSP16112 A0 AC

Call for availability of Hi-Rel parts and MIL-883C screening.